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BOEING AEROSPACE COMPANY
KENT, WASHINGTON 98124

FINAL REPORT

ANALYSIS OF FIELD USAGE FAILURE RATE DATA FOR PLASTIC ENCAPSULATED SOLID STATE DEVICES

Prepared Under:

Contract #NAS8-33079
entitled "DEVELOPMENT OF DESIGN, QUALIFICATION, SCREENING, AND APPLICATION REQUIREMENTS FOR PLASTIC ENCAPSULATED SOLID-STATE DEVICES FOR SPACE EQUIPMENT"

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1.0 INTRODUCTION AND SUMMARY

This report describes the effort performed under the first phase of a NASA contract entitled "Development of Design, Qualification, Screening, and Application Requirements for Plastic Encapsulated Solid-State Devices for Space Equipment" (NAS8-33079) for NASA/Marshall Space Flight Center. The objectives of this phase were to:

- o Gather field usage failure rate data on the reliability of plastic encapsulated semiconductors.
- o Gather data from manufacturers of plastic encapsulated semiconductors on the anticipated failure rates of their parts.
- o Determine the optimum screens suggested by the manufacturers, as necessary, to achieve high reliability at low cost.
- o Compile these data into a guide for use by NASA program managers, design managers, and parts engineers in the selection and use of plastic encapsulated semiconductors.

As a result of telephone conversations with approximately 50 users, plant visits to 14 users, and plant visits to seven manufacturers of plastic encapsulated semiconductors, a definite position can now be taken as to the viability of the use of plastic encapsulated semiconductors in selected NASA applications.

It has been found from field usage data that the reliability of plastic encapsulated semiconductors is now adequate to support their consideration for use in NASA systems, particularly in low-cost systems. By the application of strong parts engineering disciplines, the problems of the relative looseness of control of the manufacturers can be satisfactorily addressed. It is important to note tnat only part types that are in high volume continuous production may be considered under this concept. This implies that NASA should procure the plastic encapsulated devices for their applications (low volume buys) from standard manufacturers' high volume lines and apply screens (as defined later in this report) to obtain the required device performance.

Section 2 summarizes the significant findings of the program with a summary for each of the categories of reliability, manufacturer selection, qualification testing, cost, and screening. Section 3 describes the actual data search program, both at users and manufacturers of plastic encapsulated semiconductors.

Section 4 summarizes the data findings from each source, users and manufacturers. Analysis of the data findings is presented in Section 5, which covers the time-related factors of the failure rata data and incorporates the manufacturers' projections of the failure rates for different part types. Section 6 covers the cost factors determined in the course of the conversations with both the users and the manufacturers and treats both procurement costs and parts engineering costs. The unique factors of qualification invoked by the use of plastic encapsulated semiconductors are discussed in Section 7, and Section 8 treats the special screening requirements that must be considered for the development of high integrity parts for NASA applications.

This report contains four appendices. Appendix A includes the data sources that were found to be most useful in the analysis of the users data and includes much of the raw data obtained from the users. Appendix B comprises a complete selection criteria document for use by NASA project managers, designers, and parts engineers in the selection and application of plastic encapsulated semiconductors. This selection guide is a distillation of the significant findings of the main body of the report into a treatise that is intended to be usable in the field of NASA parts selection and control. Appendix C contains the bibliography. Appendix D contains the tabulated field usage data.

With the publication of this document, the objectives of the first portion of Contract NAS8-33079 have been met.

2.0 SIGNIFICANT FINDINGS OF THE PROGRAM

2.1 Reliability Summary

The reliability data obtained during this program were obtained from users of plastic encapsulated devices who had actual, documented field reliability data. There was no interest in obtaining predicted reliability from in-house reliability tests. Over one dozen users had field reliability data that they were willing to share with this program. The data were reviewed objectively and showed that these users are producing quality products with the use of plastic encapsulated devices. In addition, those users contacted that did not have field reliability data expressed overall favorable comments about the use of plastic encapsulated devices. There were no "horror stories" uncovered during these interviews with the users.

The environment in which the devices were used was, in most cases, benign Applications included telephony, computer products, commercial products, such as televisions and microwave ovens and test measurement equipment. Most of these products are utilized in air-conditioned, dry environments although some products did see high heat (microwave ovens and test equipment) and humidity (outdoor TVs and test equipment). The use of these products with plastic encapsulated devices has demonstrated that there are certain applications where these devices can be used with a high degree of confidence. Most of the users contacted intend to strive for 100% plastic encapsulated devices in their products, where practical (linear devices in the only exception).

As for NASA applications, plastic encapsulated devices may possibly be used reliably for benign environments or low cost experiments. This would be better defined as applications that allow MIL-STD-883, Class C devices (a NASA Grade 3, if established, would control the use of these devices for NASA applications). Where cost is a factor and mission success is not placed in jeopardy, plastic encapsulated devices now seem to be a possible alternative.

It should be noted that the data, to date, on the field experience of plastic encapsulated devices are not sufficient to support using these devices in all NASA applications. Grade 1 as well as Grade 2 devices should remain hermetically sealed.

An important finding of this program was that plastic encapsulated devices can be used reliably in selected applications, if selected and applied correctly. These factors are discussed in the following subsections.

2.2 Manufacturer Selection Summary

Great care must be exercised in the selection of plastic encapsulated semiconductor manufacturers to ensure that they are in continuous volume production of mature products for which they are willing to make a reliability commitment. The manufacturer must have in place an in-house reliability screening program and must establish a track record of high integrity parts which they can demonstrate when the parts are subjected to specific qualification tests.

2.3 Qualification Tests Summary

Qualification tests have been identified that meet the criteria of effectiveness and low cost. Lot qualification is not normally performed but instead a manufacturer's products are subjected to qualification testing at 9-month to 1-year intervals. Qualification tests found to be cost effective are autoclave tests, temperature cycling, and extended life test burn in. The tests must be severe enough to induce failure in a significant number of the parts so that meaningful comparisons between manufacturers can be made.

2.4 Screening Summary

Low cost reliability effective screens are available that can be performed either by the part manufacturers or by screening laboratories. Burn in and 100% electrical measurement can result in a 5:1 improvement in field usage reliability. The baseline for cost effective screening is the typical manufacturer's own in-house program such as PEP, Better, or Matrix 6. However, because of minor differences between these in-house programs, it would be desirable to establish a NASA Standard Flow for screening of each part type in the same manner, independent of the manufacturer. This NASA Standard Flow would encompass the important features of each of the in-house programs espoused by the manufacturers.

2.5 Cost Summary

In spite of the emphasis that must be placed on use of strong parts management disciplines in the application of plastic encapsulated semiconductors, the cost benefits that will result will still be significant as compared to the application

of hermetic parts. The basic plastic encapsulated part cost is three-fourths to one-half the cost of hermetic parts, and the screening costs would be significantly less than JAN screening costs if standardized simplified screening were employed. The cost factor precludes the use of custom or unique semiconductors in plastic encapsulation, since the low costs only accrue for the industry standard part types for which there is continuous production in very large quantities. Typically, the users surveyed indicated at least a 30% cost saving of screened plastic encapsulated devices as compared to the equivalent hermetic device.

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3.0 DATA SEARCH AND CONTACT

The first phase of this contract was directed towards the gathering of data on the field usage reliability of plastic encapsulated semiconductors and on the manufacturer-predicted reliability and cost of screened plastic encapsulated semiconductors. A large number of telephone calls was made to possible user data sources and supportive manufacturers, and plant visits were made to the contacts who indicated they had data or would be cooperative in the compilation of data.

3.1 Users of Plastic Encapsulated Semiconductors

The investigation of the available data on field use of plastic encapsulated semiconductors began with a thorough review of the published documentation on the subject. A list of the technical papers and articles that were read is presented in the bibliography section. From this review, a significant number of authors were identified who appeared to have data that could be applied to the definition of field usage reliability, as opposed to screening test data. A series of telephone calls was initiated that was to continue over a period of three months, to search for users who would be willing to share their data with this program. Table 1 is a list of the companies who were contacted by telephone in the course of the investigation. Only fourteen of these companies turned out to have data that could be shared. The rest of the companies could not participate in the program for a variety of reasons. Most of the nonparticipants do not have any data collection system and hence do not have any way of keeping track of the field failure rates of their semiconductor devices. Apparently in the commercial world of plastic encapsulated semiconductors, many companies find the cost of data collection to be too high for the expected benefits. However, the parts engineers in these companies usually expressed the wish that they could set up a system to track their field usage reliability performance.

Two companies indicated that they had significant amounts of field usage reliability data but their company policy would forbid them from divulging this data to any outside agencies, even in the event of promises to protect their proprietary interests. It appears that there is a fear that their competitors will use the field usage reliability to gain a competitive advantage if they were to gain access to the data. One data source who indicated that he had a significant amount of data that he was just beginning to collate later disclosed that a fire and flood

TABLE 1a: TELEPHONE CONTACTS MADE

Amdahl	Palo Alto, California
Burroughs	Downingtown, Pennsylvania
Burroughs	Plainfield, New York
Burroughs Corporation	Plymouth, Michigan
Chrysler Electronics	Huntsville, Alabama
Compugraphics	Boston, Massachusetts
Control Data Corporation	Minneapolis, Minnesota
Control Data Corp. Small Systems Division	La Jolla, California
Delco Electronics	Kokomo, Indiana
Digital Equipment Corporation	Maynard, Massachusetts
General Electric	Utica, New York
General Electric Semiconductor Products Dept.	Syracuse, New York
Harris Computer Systems	Ft. Lauderdale, Florida
Harris Data Systems	Dallas, Texas
Harris RF Communications	Rochester, New York
Harris Satellite Communications Division	Melbourne, Florida
Hewlett Packard	Palo Alto, California
Honeywell Information Systems	Phoenix, Arizona
IBM Commerical Systems	Endicott, New York
IBM Commercial Systems	Fishkill, New York
IBM Commercial Systems	Poughkeepsie, New York
IBM Federal Systems	Owego, New York
Intel Systems	Santa Clara, California
John Fluke Co., Inc.	Mountlake Terrace, Washington
Litton Microwave Ovens	Minneapolis, Minnesota
Mohawk Data Sciences	Herkimer, New York
Mostek	Carrollton, Texas
NCR	Miamisburg, Ohio
NCR	Wichita, Kansas
Polaroid Corporation	Cambridge, Massachusetts
PRD Harris	Syossett, New York
Reliability Analysis Center	Rome, New York
Sanders Associates	Nashua, New Hampshire
Sperry Flight Systems	Phoenix, Arizona
Sperry Univac Communications and Terminals	Salt Lake City, Utah
Sperry Univac Information Systems Division	Sunnyvale, California
Sylvania TV	Batavia, New York
Synertek Systems	Santa Clara, California
Tektronix	Beaverton, Oregon
Teltone	Kirkland, Washington
Teradyne	Boston, Massachusetts
Teradyne	Sunnyvale, California
Texas Instruments Systems Division	Houston, Texas
Theta Instruments	Fairfield, New Jersey
Vidar TRW	Mountain View, California
Wang Associates	Lowell, Massachusetts
Xerox	Webster, New York
Xerox Data Systems	Los Angeles, California
Zenith TV	Glenview, New York

in the factory has so disrupted the engineering operations that he would not be able to get back to start the data reduction for six months, and this contact had to be omitted.

In all cases of data discussion, the proprietary interests of the respondees were protected. The data discussions that follow have been sanitized to remove the identities of the responding companies, with the companies being coded for reference.

The field of plastic encapsulated semiconductors encompasses a large number of device types beyond the common dual-in-line packaged small scale integrated circuits such as nand gates and flip flops. Table 2 gives a breakdown of the categories of parts that were considered in the data gathering. The amounts of data that were uncovered varied from part type to part type and from user to user, and where any one category was found to have very little data available it would be combined with others to create a reasonably sized data base.

3.2 Manufacturers of Plastic Encapsulated Semiconductors

The main thrust of the contacts with the manufacturers was to define the in-house screening programs possible and to identify potential standardized screening that could be applied to plastic encapsulated semiconductors. Manufacturers' published information on their in-house screening programs (e.g., PEP, Better, A+) were studied to determine the appropriate manufacturers to visit. A letter of introduction to the problem was then sent to seven semiconductor manufacturers along with a chart that summarized the information that would be discussed on a subsequent plant visit. The letter and chart are shown in Appendix A.5.

Plant visits were then made to the seven manufacturers who were located at eleven different facilities. The emphasis in the plant visits was to find out what products were covered by the in-house screens, to define costs if possible, and to determine the resultant reliability predicted by the manufacturers. Table 1b lists the semiconductor companies that were contacted.

Fairchild Semiconductor	Mountain View, California
Intel	Aloha, Oregon
Intel	Santa Clara, California
Motorola	Austin, Texas
Motorola	Mesa, Arizona
Motorola	Phoenix, Arizona
National Semiconductor	Santa Clara, California
Raytheon	Mountain View, California
Signetics	Mountain View, California
Texas Instruments	Dallas, Texas
Texas Instruments	Houston, Texas

TABLE 1b. Semiconductor Manufacturer Plants Visited

- MICROCIRCUITS
  - Bipolar
    - SSI
      - Logic
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
      - Linear
        - Amplifier
        - Voltage Regulator
    - MSI
      - Logic
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
    - LSI
      - Logic - STTL
      - RAM
      - PROM
      - Linear
  - MOS
    - SSI - Logic - CMOS
    - MSI - Logic - PMOS
    - LSI
      - Microprocessor - NMOS
      - RAM
        - NMOS
        - PMOS
      - Logic - PMOS
      - ROM - PMOS
- TRANSISTORS
  - Bipolar
    - Small Signal
      - NPN
      - PNP
    - Power
      - NPN
      - PNP
  - FET
    - Small Signal
      - N-Channel
      - P-Channel
- DIODES - Small Signal and Zener
- SCRs

TABLE 2: CATEGORIES OF PARTS COVERED BY THIS DOCUMENT

There is a significant problem in the incorporation of the manufacturers' in-house screens into the NASA reliability assurance regime. The problem stems from the fact that each of the manufacturers performs the in-house screening on large numbers of parts and is unwilling to make any revisions to the way in which the screening is performed. However, since the screening is a little different from manufacturer to manufacturer, the manufacturers cannot meet the NASA desire to have a single part number procurable from each of several manufacturers, unless there is a custom specification written for each part type. Thus, the emphasis in the manufacturer plant visits was to define areas of agreement and reasons for disagreement in what the optimum, effective, and low cost screens should be for NASA purposes.

4.0 SUMMARY OF DATA FROM EACH SOURCE

4.1 Users

4.1.1 User A Data Findings

User A conducted a controlled measurement of the reliability of plastic encapsulated microcircuits by installing operating time meters on a number printed circuit cards so as to generate a record of the number of operating hours for each type of part before failure. The details of the program are discussed in the Appendix A.1, where the complete report of User A is reproduced. The report covers failures removed and analyzed from 490 printed circuit cards. The part types covered include SSI, MSI, and LSI microcircuits that were fabricated in 1974. The technology included standard TTL, Schottky TTL, and HTTL. Table 3 summarizes the data from the 490 metered cards, and Table 4 summarizes data that was calculated from an additional 2900 circuit cards that were not metered but were failure analyzed. These data were calculated by using additional information given to Boeing by User A during the plant visit that permitted the assessment of the number of devices of each type in each circuit card.

The large number of MSI TTL microcircuits that failed in both the metered and unmetered circuit cards were attributed by User A to the fact that one particular microcircuit manufacturer (referred to as Vendor A) did not have glassivated surfaces on his products until late in the program. As a result, there was a large number of corrosion failures that occurred. When the Vendor A switched to a glassivated product, the number of corrosion failures dropped to zero.

The data of Tables 3 and 4 have been tabulated onto a summary listing that also includes the identification of the screening the parts received and the environment in which they were used. The codes for the screening and environment are shown in Table 5. The listing is described in Appendix D.

The parts used in User A's program did not receive any screening except 25°C electrical measurement. The environment in which the parts and systems are used is a benign office environment. User A has since instituted limited screening of the type available through the part manufacturers' in-house screening programs.

TABLE 3. User A Metered Circuit Card Failure Rates

	SSI			MSI				LSI	
	TTL	STTL	HTTL	TTL	STTL	HTTL	Linear	STTL	NMOS
Plastic Encapsulated Microcircuits									
# Device Hours	1.54E7	1.88E7	1.33E8	9.67E7	2.21E7	5.1E6	1.6E6	1.6E6	----
# Failures	5	0	15	22	1	0	0	0	----
Failure Rate %/1000 hrs	0.042	.0049	.013	.025	.039	.018	.058	.058	----
Hermetic Microcircuits									
# Device Hours	2.3E6	3.6E6	2.0E7	1.5E7	3.3E6	8E5	2.4E5	3.2E6	9.3E5
# Failures	0	0	0	1	0	1	0	0	0
Failure Rate %/1000 hrs	.04	.025	.0045	.014	.028	.25	.38	.029	.1

TABLE 4. User A Unmetered Circuit Card Failure Rates

	SSI			MSI			LSI		
	TTL	STTL	HTTL	TTL	STTL	HTTL	Linear	STTL	NMOS
Plastic Encapsulated Microcircuits									
# Device Hours	1.3E8	1.1E8	7.0E8	7.3E8	1.1E8	2.3E7	7.4E6	9.6E6	----
# Failures	5	2	19	53	7	5	0	3	----
Failure Rate %/1000 hours	.005	.0029	.003	.0076	.0076	.027	.012	.044	----
Hermetic Microcircuits									
# Device Hours	1.9E7	1.5E7	1.1E8	1.1E8	1.1E7	3.5E6	1.1E6	1.4E6	4.2E6
# Failures	0	0	0	0	0	0	0	0	0
Failure Rate %/1000 hours	.005	.006	.0008	.0008	.0055	.026	.082	.063	.022

TABLE 5: CODES FOR DATA TABULATION FORMAT

Screening Code (entered in Screening Column)

Code No.	Abbreviation	Meaning
1	JA	MIL-M-38510 Class A (JAN)
2	A-1	MIL-STD-883, Method 5004 Class A
3	A-2	Vendor Equivalent of A-1
4	JB	MIL-M-38510 Class B (JAN)
5	B-1	MIL-STD-883, Method 5004 Class B
6	B-2	Vendor Equivalent of B-1
7	B-1/JB	Combination of JAN and B-1
8	B-2/N	Varying between B-2 and None
9	JC	MIL-M-38510 Class C (JAN)
10	C-1	MIL-STD-883, Method 5004 Class C
11	C-2	Vendor Equivalent of C-1
12	X	Non-Standard screen that includes Burn-in
13	None (N)	No screening beyond normal vendors QC
14	NR	Not Reported
15	D.O.	Data Omitted
16	RT	25°C Electrical Measurement Only
17	HR	Hot Rail Electrical Measurement

Environment Code (entered in Environment Column)

1	AI	Airborne, inhabited
2	AIU	Airborne, inhabited/uninhabited
3	AU	Airborne, uninhabited
4	GB	Ground, benign
5	GBC	Ground, benign, commercial
6	GF	Ground, fixed
7	GM	Ground, mobile, inhabited
8	GMU	Ground, mobile, uninhabited
9	GP	Ground, portable
10	GT	Ground, transportable
11	MRB	Missile, ground, benign
12	ML	Missile, launch and flight
13	NS	Naval, sheltered
14	NSS	Naval, submarine
15	NU	Naval, unsheltered
16	SF	Satellite, flight
17	SL	Satellite, launch
18	SPL	Spacecraft, launch and flight

4.1.2 User B Data Findings

This user must use parts in an application that represents a fairly severe environment: ground, mobile, inhabited. In addition, there are severe pressures to ensure high customer satisfaction with extremely low failure rates required. Table 6 shows the failure rates being achieved by this user in the first year of field usage of his parts (warranty returns). These failure rates are being achieved on very large numbers of parts: usage quantities of microcircuits are on the order of 180 million parts per year. Five and a half million systems were sold in 1977 alone. User B feels that the second year of usage will see these failure rates decrease by a factor of two. All parts receive a 100% hot rail test, and in addition, their part manufacturers must perform periodic lot qualification tests such as 24-hour autoclave tests. This user meets quarterly with his manufacturers to discuss lot rejections, line removals, and field removals.

4.1.3 User C Data Findings

User C employs an extensive data gathering system to track the failure rates for 16 different types of semiconductors. Not all of the detailed data was obtained, but User C did provide detailed data on eleven of the device types in both plastic and hermetic configurations. The data are gathered from warranty returns and are based on an average annual operating time for each system of 2400 hours. The parts used by User C do not receive any type of screening at all except for what the manufacturers perform on their own.

Table 7 summarizes the field usage warranty removal data that were provided by User C. The actual data sheet from which these data were obtained is reproduced in Appendix A.2. The data are collected every six months so that the trends of the removal rates can be plotted, as shown in the curves plotted and reproduced in Appendix A.2. Table 7, however, only summarizes the data every year over the last half of 1976, all of 1977, and the first half of 1978. From the data, User C feels that n-channel FETs are not acceptable in plastic and that variable voltage regulators would be undesirable in plastic.

4.1.4 User D Data Findings

The parts discussed with User D were not of the conventional novolac plastic encapsulation. Instead they were of the polymer sealed configuration in which the ceramic package (air cavity) is assembled using organic polymer material for

TABLE 6. User B Field Usage Failure Rate Data

Year	Part Type	Package	Device Hours	Failure Rate
1977	Germanium Power Transistor	Hermetic	3.6×10^9	.03%/1000 hrs.
1977	Small Signal NPN Transistor	Plastic	2×10^9	.01%
1977	Axial Lead Diode	Plastic	2.8×10^9	.0074%
1978	Light Emitting Diode	Plastic	1.1×10^9	.012%
1977	PMOS LSI	Plastic	2.0×10^8	.25%
1978	PMOS LSI	Plastic	2.0×10^8	.016%
1977	Bipolar Linear SSI	Plastic	8.1×10^9	.05%
1977	Bipolar Fixed Power Regulator	Plastic	2.2×10^9	.11%
1977	Bipolar Power Audio Amplifier	Plastic	4×10^7	.05%

TABLE 7. User C Removal Rate Data

Part Type	1976 Parts (Data 5/77) Fails prev. 6 mo.	Device hrs.	Failure Rate %/yr. (2400 hr.)	%/ 1KHR	1977 Parts (Data 5/78) Fails prev. yr.	Device hrs.	Failure Rate %/yr. (2400 hr.)	%/ 1KHR	1978 Parts (Data 11/78) Fails prev. 6 mo.	Device hrs.	Failure Rate %/yr. (2400 hrs.)	%/ 1KHR
Transistor SS-NPN (H)	335	1.44E9	.0592	.025	703	2.92E9	.0576	.024	396	1.60E9	.0595	.025
Transistor SS-NPN (P)	598	3.55E9	.0404	.017	1093	7.0E9	.0384	.016	468	3.62E9	.0310	.013
Transistor SS-PNP (H)	315	1.15E9	.0659	.027	585	2.25E9	.0624	.026	280	1.13E9	.0595	.025
Transistor SS-PNP (P)	550	2.44E9	.0541	.023	1041	4.95E9	.0504	.021	460	2.66E9	.0415	.017
Transistor SS NFET (H)	94	3.37E8	.0670	.028	356	7.0E8	.1424	.051	182	4.10E8	.1066	.044
Transistor SS NFET (P)	173	2.13E8	.1951	.081	339	3.95E8	.2064	.086	152	2.01E8	.1814	.076
Transistor SS PFET (H)	0	1.87E7	---	.005	2	1.35E7	.0720	.030	0	7.85E6	---	.012
Transistor SS PFET (P)	29	9.2E7	.0755	.031	35	1.1E8	.0792	.033	23	5.54E7	.0997	.042
Transistor Pwr NPN (H)	188	2.91E8	.1553	.065	390	5.95E8	.1584	.066	274	2.80E8	.2346	.098
Transistor Pwr NPN (P)	146	1.89E8	.1855	.077	246	3.8E8	.1560	.065	87	1.73E8	.1204	.050
Transistor Pwr PNP (H)	32	6.85E7	.1121	.047	131	1.5E8	.1320	.055	44	7.31E7	.1445	.060
Transistor Pwr PNP (P)	56	9.68E7	.1388	.058	68	2.0E8	.1600	.034	38	1.06E8	.0858	.036
SSI Linear Op Amp (H)	393	7.66E8	.1231	.051	726	1.45E9	.1200	.050	304	7.72E8	.0944	.039
SSI Linear Op Amp (P)	59	8.66E7	.1635	.068	139	1.8E8	.0624	.026	24	1.09E8	.0529	.022
Voltage Reg - Fixed (H)	30	3.33E7	.2164	.090	50	4.45E7	.1488	.062	35	5.03E7	.1669	.070
Voltage Reg - Fixed (P)	38	4.13E7	.2220	.092	112	1.11E8	.2472	.103	33	7.36E7	.1075	.045
Voltage Reg - Adj. (H)	147	1.20E8	.2932	.122	296	2.63E8	.2688	.112	118	1.18E8	.2407	.100
Voltage Reg - Adj. (P)	20	6.25E6	.7685	.320	44	1.47E7	.7152	.298	16	1.14E7	.3359	.140
SSI ECL (H)	11	1.67E7	.1585	.066	26	6.8E7	.0912	.038	35	1.00E8	.0837	.035
SSI ECL (P)	38	9.26E7	.0985	.041	70	2.5E8	.0696	.029	51	2.46E8	.0498	.021
SSI/MSI CMOS (H)	20	3.59E7	.1337	.056	34	1.07E8	.0792	.033	25	8.14E7	.0737	.031
SSI/MSI CMOS (P)	101	3.54E8	.0685	.029	170	6.8E8	.0600	.025	99	4.11E8	.0578	.024

the sealant. In this sense, the technology of polymer sealed devices is different from plastic encapsulation, in that there is no encapsulant in intimate contact with the surface of the silicon dice. However, from the standpoint of the effect of moisture on the reliability of the parts, the polymer sealing process presents the same problems as the plastic encapsulation.

The parts for which data were obtained were multichip random access memories; 8 chips were used per module, and each module (a 1" square polymer sealed package) thus incorporated from 12K to 25K bits of memory. The parts were screened by User D (the manufacturer) with a burn in of undetermined configuration. The environment in which they were used was an office environment. Table 8 summarizes the data that were obtained from User D covering several different time periods.

4.1.5 User E Data Findings

This user employs four basic microcircuits in his small systems which are sold in the 5 to 6 million quantity annually. Because the electronics operates only seconds per year, the primary operating environment is storage. The environment that the systems see is not benign but may run a wide range of temperatures and humidities. In spite of this, User E has experienced so few semiconductor failures that they do not even bother to track the failures. In all the time that they have been using electronics in their systems, there has only been one failure that could be attributed to the plastic encapsulation. The rest have all been due to conventional die-related problems. This may result from the fact that User E requires qualification testing to be performed every 9 months to control the manufacturer of their microcircuits, and performs 100% electrical measurement of the circuit assemblies as an incoming inspection.

4.1.6 User F Data Findings

User F shared the data they had gathered for an electronic system that uses a large amount of plastic encapsulated microcircuits. An in-house test was recently conducted on ten of these systems for 1000 hours to gather reliability information. Although the data were not from actual field usage, they were derived from simulated field usage of the complete systems, and are thus flet to be applicable. The parts in the system were all bought in 1978 from local distributors with no qualification testing performed. All parts were electrically measured at 25°C and one circuit type (of the type for which the one failure occurred) was subjected to a 168-hour

TABLE 8. User D Failure Rate Data

Year	Model	Memory Type	No. of Device Hours	No. of Failures	Failure Rate %/1000 Hours
1973	Adv. Development	12K (8 chips)	1.458E6	0	.062
1974	Adv. Development	25K (8 chips)	1.463E6	0	.062
1975	Service Test and Small Processing System	25K (8 chips)	9.243E5	1 (a)	.22
1973	Adv. Development	12K (8 chips)	8.748E6	25 (b)	.31
1974	Adv. Development	25K (8 chips)	8.778E6	17 (b)	.20

(a) Not Seal Related

(b) Page Failure, but not all analyzed. Repair action did not preclude failure being caused by RAM

burn in. Table 9 summarizes the results of the test. These data were obtained by analysis of the make-up of each of the circuit cards in the system. User F had established the categories shown in Table 9. The quantity of each circuit card that was used in the system was then multiplied by the number of parts in each category to obtain the total number of parts used. The cause of failure of the CMOS part was not determined.

4.1.7 User G Data Findings

This user has the best data collection system known for the tracking of warranty returns on all electronic parts used in field deliverable systems. User G employs a computerized system to track the reliability performance on over 9000 part numbers on a month-by-month basis, and they are able to compute and identify the removal rate for any part in use over the last three years. They estimate that their systems are in use an average of 1000 hours per year, so the removal rate in percent per year translates directly into percent per 1000 hours.

Approximately half of the removals are failure analyzed and the results show that approximately 2/3 of the removals are verified failures.

Only a small amount of the large available data base was recorded for this program. An entire morning was spent at User G recording the data on just certain basic part types that corresponded to the parts also reported by User C. Only the most highly used part types were recorded, resulting in 23 sets of data shown in Table 10. The quantities of each part used by User G range from 50,000 to 1,000,000 parts per year, so the data represent a large number of part hours. The data for each year were obtained by looking at the December printout, using the assumption that the cumulative parts tabulated in that month were of the vintage of that year.

User G generally does not use any screening other than 100% electrical measurement at 25°C at incoming receiving inspection. The 25 high volume part types are 100% tested but many other part types are not. The environment that the systems are used in is a benign office or laboratory environment.

This user represents an extremely valuable data source, and if it were necessary to generate additional data it would be wise to investigate the possibility of researching this data source at greater length to analyze the other part types

TABLE 9. User F Failure Rate Data - 1978 Parts

Circuit Type	Number per System	Device Hours	Failures	Failure Rate %/1000 Hours
SSI Gate TTL	2072	2.1×10^7	0	.0044
SSI Flip Flop TTL	545	5.5×10^6	0	.017
MSI Gate TTL	768	7.7×10^6	0	.012
MSI Flip Flop TTL	663	6.6×10^6	0	.014
Linear Amplifier	339	3.4×10^6	0	.027
LSI RAM NMOS	330	3.3×10^6	0	.028
LSI PROM Bipolar	838	8.4×10^6	0	.0105
SSI CMOS Gate	28	8.4E5	1	.24

PART NUMBER	PART CLASSIFICATION	1976		1977		1978	
		DEVICE HRS	R/R	DEVICE HRS	R/R	DEVICE HRS	R/R
2N3904	TO-92 Transistor NPN SS (<100v)	1.4×10^9	.0238	1.8×10^9	.0197	2.3×10^9	.0146
2N5551	TO-92 Transistor NPI SS (>100v)	3.2×10^8	.085	4×10^8	.080	5×10^8	.063
TIP31A	TO-220 Transistor NPN PWR (<100v)	6.2×10^6	.022	1.2×10^7	.059	1.2×10^7	.069
TIP47	TO-220 Transistor NPN PWR (>100v)	1.6×10^7	.053	1.5×10^7	.23	2.5×10^7	.127
2N2219	TO-39 Transistor NPN SS (<100v)	7.2×10^7	.096	8×10^7	.043	1×10^8	.03
2N3439	TO-39 Transistor NPN SS (>100v)	7.8×10^7	.129	8.2×10^7	.098	1×10^8	.105
2N2222	TO-18 Transistor NPN SS (<100v)	5.3×10^7	.022	7×10^8	.0215	9.4×10^8	.019
C106B2	SCR	1.6×10^7	.092	1.8×10^7	.116	1.9×10^7	.09
	Plastic N-Channel JFET	1.1×10^8	.131	1.2×10^8	.126	1.6×10^8	.075
	Metal N-Channel JFET	8×10^6	.032	2.0×10^7	.065	2.1×10^7	.026
	TO-220 5v Fixed Volt Req (Plastic)	1.4×10^7	.127	1.7×10^7	.12	2.7×10^7	.073
	Variable Voltage Req. (Ceramic)	4.8×10^7	.195	4.5×10^7	.17	5.9×10^7	.124
74LS00	SSI Gate Low Power Schottky	3.8×10^7	.01	1.0×10^8	.005	2.0×10^8	.002
74LS74	MSI FF Low Power Schottky	3.6×10^7	.013	$.8 \times 10^8$	.008	2.0×10^8	.005
7400	SSI Gate Standard TTL	3.4×10^8	.021	3.5×10^8	.020	4.6×10^8	.03
7474	MSI FF Standard TTL	2.4×10^8	.024	2.3×10^8	.021	3.2×10^8	.0235
74S00	SSI Gate Schottky TTL	3.6×10^7	.017	4.5×10^7	.018	8.1×10^7	.02
74S74	MSI FF Schottky TTL	5.4×10^6	.04	1.5×10^7	.007	2.2×10^7	.0142
10102	SSI Gate ECL (Hermetic)	3.9×10^7	.039	6×10^7	.031	7.5×10^7	.039
10131	MSI (Hermetic)	2.9×10^7	.10	7.2×10^7	.033	7.8×10^7	.044
LM741	SSI Op Amp Linear	3.0×10^8	.101	3×10^8	.067	3.9×10^8	.0867
2102	LSI 1K Static RAM NMOS	5.2×10^7	.06	1.2×10^8	.07	1.0×10^8	.055
μP6800	LSI NMOS Microprocessor	-----	-----	1.1×10^7	.05	1.4×10^7	.157

TABLE 10. User G Failure Rate Data

that are logged. When one considers that the removal rate for over 9000 part types is tracked every month, the data analysis possibilities are staggering.

User G does employ a considerable amount of lot qualification testing to ensure that high integrity lots are being shipped. The primary test used for qualification testing is accelerated stress testing. Burn in of 150°C is commonly used and for linears it has been found that a high voltage stress life test with a 24-volt differential applied to the inputs gives an acceleration factor of 1000.

4.1.8 User H Data Findings

This user is a small company that manufactures a complex small system for use in an office environment. They have data on all failures that have been sent back by field service including the number of hours on the system at the time of failure. Table 11 shows the distribution of failures reported in the last three months of 1977. Data were obtained from User H on the reliability performance of two different versions of their system. The first set of data resulted from parts that were of the 1976 vintage and were installed in the older model of their system that has been in continuous production since 1974. In fact over 100,000 units of the older design have been sold. The data resulting from the 1976 vintage parts are shown in Table 12. This table also shows data resulting from 1977 vintage parts that were installed in a newer model of the system. Data taken as of October, 1978, provided 8 months of operating life experience, resulting in 32,546 service months.

User H subjects all parts to a 100% hot rail electrical measurement at incoming inspection.

4.1.9 User J Data Findings

This user manufacturers an electronic system that gets installed into an office environment. Two different versions of the equipment have been developed. The first was originally built in the 1973 time frame and used older circuit technology. The second was built in the 1975 time frame and uses some newer circuit types such as low power Schottky. Data from all of the installed systems have been collected, providing an extremely large number of part hours as a data base. Table 13 summarizes the data that were collected as a result of the plant visit. The PMOS LSI parts are all hermetically sealed ceramic packages. The linear SSI parts are

TABLE 11. User H Failure Modes Found October-December, 1977

LSI Chip Failures	10%	
CR8 Diode Failures	10%	
Diodes (Other than CR8)	3%	
Transistor Failures	9%	
820 pF Silver-Mica Capacitors (Drift)	8%	
Capacitors (other than 820 pF)	3%	
CMOS Device Failures	5%	
Op Amp Failures	3%	
Potentiometers Intermittent, etc.	5%	
Line-Split Relay Contact Welding	9%	14%
Line-Split Relay Coil, Timing, etc.	5%	
Pulser Relay Failures	4%	
Battery-Feed Relay Failures	3%	
Resistors	2%	
Workmanship/Quality Problems	5%	8%
Mechanical (Broken Wires, etc.; possible, but not definite Workmanship/Quality Problems)	3%	
Fuses	2%	
Miscellaneous	2%	
No Trouble Found	11%	

TABLE 12. User H Failure Rate Data

Year	Part Type	#/Module	Module Hours	Device Hrs	# Failures	Failure Rate %/1KHR
1976	SSI CMOS	7	3.6E8	2.52E9		.004
1976	40-Pin Custom PMOS LSI	1	3.6E8	3.6E8		.045
1976	SSI Linear Op Amp (single) 741	10	3.6E8	3.6E9		.001
1976	SSI Linear Op Amp (dual) 1458	11	3.6E8	4.0E9		.002
1976	Transistor SS NPN	8	3.6E8	2.9E9		.0045
1976	Transistor SS PNP	8	3.6E8	2.9E9		.0045
1976	Diodes Small Signal & Zener	47	3.6E8	1.7E10		.001
1977	SSI CMOS	2	2.56E7	5.1E7	4	.0026
1977	LSI PMOS	2	2.56E7	5.1E7	31	.065
1977	SSI Linear Op Amp (dual) 1458	8	2.56E7	2.0E8	4	.010
1977	Transistor SS NPN	5	2.56E7	1.3E8	6	.0026
1977	Transistor SS PNP	5	2.56E7	1.3E8	6	.0026
1977	Diode Small Signal & Zener	34	2.56E7	8.7E8	28	.0016

TABLE 13. User J Removal Rate Data

Year	Part Type	# Failed	Device Hours	Failure Rate 60% Confidence Level %/1000 hours
1973	Diode, Power	62	1.90 E9	.0034
	Diode, Switching	1571	2.7 E11	.00058
	Diode, Reference	337	5.6 E8	.062
	Diode, Zener	6	4.0 E8	.0018
	Diode, Light Emitting	8	9.1 E8	.0010
	Diode, Bridge Assembly	0	1.1 E8	.00089
	Transistor SS NPN	456	4.6 E9	.010
	Transistor Power NPN	68	5.6 E8	.013
	Transistor Power PNP	100	4.5 E8	.023
	Transistor SS PNP	102	3.6 E8	.029
	Photo Isolator	611	2.0 E9	.030
	SSI LTTL	656	1.4 E10	.0047
	SSI TTL	807	9.1 E9	.0090
	MSI LTTL	242	3.7 E9	.0066
	MSI TTL	351	3.1 E9	.012
	LSI PMOS (1404, 1101)	236	2.3 E9 (Hermetic)	.011
	SSI Linear Volt. Reg. Fixed	307	2.8 E9	.011
1975	SSI TTL	0	1.02 E6	.090
	MSI TTL	0	5.78 E6	.016
	SSI STTL	0	1.77 E6	.052
	SSI LSTTL	0	1.80 E7	.0051
	SSI Linear	0	4.0 E6	.023
	LSI PMOS (1404, 1101)	0	4.2 E6 (Hermetic)	.022
	SSI Linear	0	4.0 E6 (Hermetic)	.023

half plastic encapsulated and half hermetically sealed. No difference in failure rate has been observed between the two packages. The 1973 parts were not screened other than for 25°C electrical measurement, but for the 1975 parts, extensive parts control procedures were instituted, including the use of 168-hour 125°C burn in. This user employs extensive lot sampling tests on incoming part types, with a pressure pot test being the primary separator. They measure the median time to failure in a 96-hour pressure pot test and look for corrosion.

One additional point in the User J success story is that they invoke strict tests and inspections of the completed circuit cards and complete systems to weed out the early failures before they are installed on the customers' facilities. Thus, the removal rates in Table 13 result from the use of strict parts engineering disciplines for the entire system assembly process.

4.1.10 User K Data Findings

This user has field failure rate (removal rate) data on plastic encapsulated microcircuits that are removed from circuit cards in the first year after introduction of a new system. Sixty-one systems were monitored for one year. Each system employed 400 microcircuits and was turned on 16 hours per day, 21 days a week. Thus, approximately 98,000,000 device hours were accumulated in the first year of operation. These device hours were about evenly split between CMOS SSI and TTL SSI parts. Seven CMOS parts and 6 TTL parts were removed from the systems in the year's time resulting in the following failure rates:

CMOS: 49,000,000 device hours, 7 failures, 0.017%/1000 hours failure rate

TTL: 49,000,000 device hours, 6 failures, 0.015%/1000 hours failure rate

The systems are used in a benign office environment. The screening to which the parts are subjected consisted of the part manufacturers' standard in-house reliability screening such as PEP or A+. In addition, User K performs extensive qualification testing and monitoring of the manufacturers to maintain the integrity of the plastic encapsulated devices. In the LSI area, User K insists on 100% burn in of plastic encapsulated microcircuits, and has found that the reliability of plastic encapsulated devices is better than for the ceramic packaged devices because they are more rugged and can take normal handling with less package breakage.

4.1.11 Other Data Sources

Significant data were obtained from sources other than those associated with direct plant visits to users of plastic encapsulated microcircuits. The most voluminous of these was the Reliability Analysis Center at RADC, and other data were found by telephone contact to semiconductor manufacturers who identified customers of theirs who had given them data. Finally, the literature search uncovered one source of published data.

Reliability Analysis Center

RAC publishes several documents that summarize the experience reported by numerous companies and agencies in testing and reliability measurement of microcircuits. The two documents most applicable to this study are MDR-8, Digital Failure Rate Data, and MDR-7, Memory/LSI Data. A personal visit was made to RAC to discuss the availability of any additional data that might have become known since the last editions of these two documents, and it was found that RAC had new data that could be shared. A handwritten copy of the data new since MDR-8 was received, and proved to be quite useful because it could be assumed that the parts listed were of a 1977 vintage, whereas the data listed in MDR-8 does not have any indication of the date of the parts reported. A tabulation of the data in this handwritten data set was made to sort out the various technologies (e.g., TTL, STTL, etc.) and the various complexities (SSI, MSI, etc.). Table 14 sumarizes this tabulation and represents a summation of the device hours and failures for each of the categories listed. This was necessary because in many cases the number of device hours was less that 10^6 with zero failures, which gives an erroneously large failure rate. By combining all of the device hours and failures for each category a realistic picture of the overall reliability for each category could be established. The complete handwritten set of data is reproduced in Appendix A.3.

It was also found that a complete update of MDR-7 (Memory/LSI Data) is in the works and RAC provided a computer printout of the data that will be published. The 220 page printout was analyzed for entries labelled "FIELD" that had plastic encapsulated devices called out. Twenty-nine entries were found, plus 8 more that covered hermetic devices. These are listed on Table 15.

TABLE 14. RAC-Reported Data on 1977 Digital Logic

Package	Device Technology	Screen	Environment	Device Hours	# Failures	Failure Rate %/1000 Hours
Plastic	LSI PMOS	13	7	2.4 E8	67	.029
Plastic	SSI STTL	12, 13	4	6.8 E6	0	.014
Plastic	SSI LSTTL	12, 13	4	1.3 E6	0	.07
Plastic	SSI TTL	12, 13	4	5.5 E6	0	.017
Plastic	MSI STTL	13	4	1.1 E7	16	.019
Plastic	MSI LSTTL	12, 13	4	2.3 E7	0	.004
Plastic	MSI TTL	13	4	3.2 E6	3	.13
Plastic	MSI TTL	12	4	4.9 E6	0	.019
Hermetic	SSI STTL	5	6, 10	4.4 E6	0	.021
Hermetic	SSI TTL	4	6, 10	7.4 E7	1	.0027
Hermetic	SSI TTL	5	3	1.7 E7	1	.012
Hermetic	SSI TTL	6	3	5.8 E6	5	.11
Hermetic	SSI TTL	10	2	1.7 E7	3	.025
Hermetic	SSI TTL	13	7	2.6 E6	0	.036
Hermetic	MSI STTL	5	7, 10	2.4 E6	0	.038
Hermetic	MSI TTL	5	3, 6, 10	4.8 E7	0	.0019
Hermetic	MSI TTL	6	3	1.3 E6	1	.16
Hermetic	MSI TTL	4	6, 10	8.3 E7	0	.0011
Hermetic	MSI TTL	10	2, 3	3.4 E7	7	.025
Hermetic	MSI TTL	13	7	1.7 E6	0	.054

TABLE 15. RAC-Reported Data on Memories & Microprocessors

Package	Year	Device Technology	Part Number Type	Screen	Environment	Device Hours	# Failures	Failure Rate %/1000 Hours
Plastic	76	MSI STTL		13	5	5.2 E7	17	.036
Plastic	77	MSI LSTTL	25L315/2907	12	5	2.6 E6	0	.036
Plastic	76	LSI ECL	1307 PROM	13	5	8.8 E6	1	.023
Plastic	76	LSI NMOS	2102 RAM	13	5	1.2 E6	0	.076
Plastic	77	LSI NMOS	4096 RAM	13	5	6.4 E6	2	.049
Plastic	76	LSI PMOS	5007 S/R	13	5	2.5 E7	28	.12
Plastic	71	MSI PMOS		13	9	2.6 E9	1321	.052
Plastic	76	LSI NMOS	3850/3851 µP	12	9	4.3 E7	462	1.1
Plastic	77	LSI NMOS	Z80 µP	13	5	4.7 E6	6	.16
Plastic	76	LSI CMOS	4020 Counter	13	5	4.5 E6	0	.021
Hermetic	76	MSI STTL	3207A	13	5	3.5 E6	0	.026
Hermetic	76	LSI PMOS	5009	13	5	1.2 E7	16	.15
Hermetic	76	LSI PMOS	1013	13	5	1.0 E7	9	.11
Hermetic	75	LSI PMOS	---	13	6	1.8 E7	22	.13
Hermetic	77	LSI NMOS	4096 RAM	13	5	3.1 E6	4	.17

Singer Business Machines

Telephone contact with one manufacturer of plastic encapsulated microcircuits resulted in the information that Singer Business Machines had performed some research on the field use reliability of plastic devices and had published the data. A copy of the paper is included in Appendix A.4. The data from this paper are also reported by RAC in MDR-8. Table 16 summarizes the significant data from this paper. The data are interesting because they are from the 1972 vintage and thus antedate the period of the widespread use of the novolac plastics. Yet even in this case the plastic parts do not show any difference in failure rate between hermetic parts and plastic encapsulated parts.

User L

The same microcircuit manufacturer also disclosed data from a major commercial system manufacturer whose systems are subjected to a very severe environment. These 1977 vintage parts were screened by the IC manufacturer to his in-house reliability screening program that included temperature cycle, burn in, and electrical measurement at 25°C and 100°C. He reported that the parts (SSI linear microcircuits) had accumulated 52 million device hours with a failure rate of .0079%/1000 hours.

Sanders Associates

The literature review turned up a paper* by Sanders Associated that had data on field usage failure rates for plastic encapsulated microcircuits. Table 17 summarizes the data from this paper. Again, the vintage of the parts is 1972, which is very early for the considerations of this report.

4.2 Summary of Data From Each Manufacturer

4.2.1 Manufacturer (1) Integrated Circuits Division (Bipolar Products)

Manufacturer (1) presented the optimal screens for digital bipolar ICs (SSI, MSI). They have found that a 145°C 40-hour burn in is very effective, especially when combined with temperature cycling from -25 to 150°C. The burn in should be static, not dynamic, to save money; static burn in is good for uncovering migration and inversion problems. The most effective screen for digital parts, however, is

*J. J. Harrahy, "Assessment of Plastic, Commercial Grade IC Failure Rates Achieved in Field Operation", Proceedings of the Symposium on Plastic Encapsulated/Polymer Sealed Semiconductor Devices for Army Equipment, May 10-11, 1978, Ft. Monmouth, NJ.

TABLE 16. Singer Business Machines Field Usage Data (1972 Parts)

Part Classification	Screening	Environment	Package	Device Hours	Failure Rate %/1000 Hours
SSI TTL	12	4	Hermetic	1.5 E7	.028
SSI TTL	12	4	Hermetic	9.9 E6	.054
SSI TTL	17	4	Hermetic	4.7 E6	.043
SSI TTL	12	4	Plastic	3.3 E6	.028
SSI TTL	12	4	Plastic	8.4 E6	.024
SSI TTL	17	4	Plastic	1.5 E7	.022

TABLE 17. Sanders Associates Field Usage Data (1972 Plastic Encapsulated Parts)

Part Classification	Screening	Environment	Device Hours	Failure Rate %/1000 Hours
SSI TTL Gate	16	6	1.9 E9	.012
SSI TTL FF	16	6	3.2 E8	.022
MSI TTL Gate	16	6	1.7 E8	.023
MSI TTL FF	16	6	5.6 E8	.022
SSI Linear	16	6	1.6 E7	.028
LSI PMOS ROM	16	6	5 E7	.0078
LSI PMOS Char Gen	16	6	8.2 E6	.029
LSI PMOS S/R	16	6	1.6 E7	.041
LSI PMOS RAM	16	6	5.0 E8	.019
LSI Bipolar RAM	16	6	4.1 E6	.128

temperature cycling which uncovers bad bonds. Manufacturer (1) feels that at least 30 cycles should be used, even though their in-house plastic reliability program uses only 10 cycles. There is a severe penalty in deviating from 10 cycles from -25°C to +150°C because that is the way their offshore production facilities are set up and deviation requires the work to be done onshore.

It was felt that double testing of digital bipolar ICs (repeating electrical tests to weed out testing escapes) would not be particularly effective, but would not be costly either. The data show the reject rate to be .8% on first test and .5% on second test.

Thermal shock (0°C ice water to 100°C boiling water) should not be allowed as a screen because Manufacturer (1)'s data shows that reliability is degraded by the shock: corrosion is made worse in 10,000-hours tests.

Manufacturer (1) discussed the optimal screens for linear bipolar microcircuits. They said the most severe problem in linear ICs is the effect of high voltage on reliability and hence a static burn in is the best screen for linears. They should be burned in at 145°C for 40 hours, or some other temperature that would keep the junction temperature at 155°C. The use of overvoltage screens (zero time screens) are not effective with linears because often the linears have onboard voltage regulators that absorb any overvoltage. So normal voltage combined with high temperature is best. Temperature cycling is also valuable and, combined with (preceding) burn in, the reliability is maximized. However, linears with Bi Fet technology cannot be operated at high temperatures. For linears, it appears that tne burn-in screen must be tailored to the individual processes, rather than applying blanket rules. Static burn in is also preferred for linears over dynamic burn in. Double testing was felt to be very effective for linear ICs.

Manufacturer (1) then developed approximate cost adders for performing reliability screening above and beyond the in-house screening which has a cost adder of 15¢ per part. A fundamental point was made in the approach to NASA plastic parts, in that a standardized specification should be written for use by all contractors with no deviation, so that quantities of mixed parts could be increased. The digital cost adders reflect such an assumption while the linear cost adders assume a nonstandard flow for the NASA screening. See Table 18.

TABLE 18. Manufacturer (1) Screening Data

	Screen	Mfr. (1) In-House Screening	NASA	Based on Standardized Flow For NASA Digital IC	Based on Nonstandard Flow Linear IC
	Temp Cycle	10 cy - 25/150°C	30 cy - 25/150°C	$.10	$.50
	Functional and DC Parameters	-----	100°C	.05	.15
	Burn In (Static)	40 hrs @ 145°C	87 hrs @ 145°C	.10	.15
	Post Burn In Test				
	Functional & DC	25°C	25°C	No charge	No charge
Repeat	Functional & DC	----	25°C	.04	.15
Repeat	Functional & DC	----	100°C	.05	.15
Repeat	Functional & DC		100°C	.05	.15
	TOTAL COST	$.15		$.39	$1.25

For LSI devices such as bipolar memory or bipolar microprocessor devices, the cost would be obtained by merely doubling the cost of the part. Thus, the adder for a $4.00 part would be $4.00 and for a $25 part the adder would be $25.

The digital ICs would have a post burn-in percent defective allowable (PDA) of 10%. The linear parts would not be subject to PDA; Manufacturer (1)'s linear organization does not have any system for working the PDA operation.

4.2.2 Manufacturer (1) Discrete Semiconductor Division

The in-house screen program is not used with discrete semiconductors. The one most effective reliability screening test for zener diodes is a 100% surge test of 100ms, 20 watts (or so) followed by 100% V_Z and I_R measurement. This test catches oxide faults. This test is not performed on plastic zeners unless required by customers. The only 100% screen test performed at present is a 25°C electrical measurement of zener diode parameters. Burn in at full rated power for 48 hours is another highly effective screen that could be imposed. However, this has a $5000 minimum lot charge plus $1 per part. Thus for small lots (say 1000 parts), the cost per part would be prohibitively expensive. The surge test can be performed for a 5¢ per part adder. Double measurement would add 5¢ per part for each temperature/measurement cycle.

The failure rate for zeners is felt to be 0.1%/1000 hours at full rated power. The application of the surge test would reduce this to 0.05%/1000 hours, and burn in would result in several orders of magnitude of improvement.

Operation of zeners at derated power is the preferred way to achieve improved reliability, using a 1.0ev activation energy applied to the junction temperature.

For rectifiers Manufacturer (1) routinely performs a 100% double voltage dc test (100 volt rectifiers are tested at 200 volts). There really isn't an optimum screen for rectifiers. Instead, the application determines the preferred screen. For DC blocking applications, an HTRB (high temperature reverse bias) test would be good, but HTRB would not be important for AC rectifying applications.

Double testing was not felt to be a useful test because Manufacturer (1)'s escape rate for rectifiers at final test is only 0.08%, including marginal parameters and

the catastrophic escape rate is only 0.001%. The immense quantities of rectifiers that must be tested works against the use of double testing because of limitations in additional throughput capability.

The standard tests performed on power transistors include 100% DC tests at 25°C and 100% test of the safe operation area (SOA) as exemplified by second breakdown. The SOA test detects bad die-attach devices and is much more effective than power burn in, which is not performed. In fact, since Manufacturer (1) does not perform burn in of power transistors, they do not have experience on its effectiveness.

Manufacturer (1) is not facilitated to perform burn in in-house. Double testing is performed (effectively) on all parts which are tape-and-reel packaged, once at final test and once after mounting on the tape. Other parts cannot be double tested in production but would have to be tested onshore by Manufacturer (1)'s Q.C.

Another effective test applied to power transistors is a power V_{BE} test, which uses a 3 amp, 3 μsec pulse through the base-emitter junction, with measurement of the resultant V_f giving good indication of wirebond integrity.

The failure rate on outgoing power transistors is predicted to be 0.1% per thousand hours at full rated power. No cost adders were given because Manufacturer (1) cannot perform any of the additional tests desired in production. However, the V_{be} test and the SOA test should be called out in any NASA specification.

For small signal transistors (TO-92 packaged), Manufacturer (1) normally performs 100% temperature cycling (7 cycles from +25° to +150°C) and 100% measurement of DC parameters.

It was determined that several additional tests could be performed 100% at a minimal cost of 5¢ per part for each screen. These are double measurement of DC parameters, measurement of the power V_{be} (forward), measurement of ΔV_{BE} on (for two different base currents - measures die attach integrity), and 100°C hot continuity test.

It was mentioned that the TO-92 transistors (small signal) use novolac plastic, but the power transistors and axial lead diodes and rectifiers use silicone encapsulant.

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The in-house screening program contains a requirement for 10 temperature cycles from 0°C to 100°C. They feel that expansion to -25/150°C would not achieve anything useful and would be very difficult to perform; since offshore production screening uses the narrower temperature range, the wide temperature range would require performing the tests onshore, resulting in special handling charges.

Burn in is performed at 155°C for 21 hours and uses a 0.96ev activation energy for the acceleration factor. Because hand wire bonding has now been replaced completely by automated wire bonding, bond defects have been reduced by two orders of magnitude.

In discussing multiple testing of functional and DC electrical parameters, Manufacturer (2) said that statistically each pass through electrical test catches 92% of the defects. So if the defect rate were 2%, 0.16% of the parts would still be defective after one pass and .013% would still be defective after two passes. They feel that because they impose a 2% PDA after burn in, double screening would not be necessary, particularly in view of the fact that a 0.1% AQL is imposed by QC on a sampling basis before lots are shipped. A 0.1% AQL translates to a 0.14% defective rate allowable. The discussion resulted in postulating that perhaps the NASA reliability process document could call for either redundant function/DC parameter testing or .1% AQL, at the manufacturer's option. No other manufacturer uses this low an AQL (0.1%) or this low a PDA (2%).

Overvoltage testing was discussed. Manufacturer (2) imposes a 100% overvoltage test at wafer probe except for Schottky and MOS products. It was felt that imposition of overvoltage testing on TTL devices would be acceptable (7 volt V_{CC} for 20ms) as a screen for oxide faults after burn in.

Manufacturer (2) then discussed reliability screening of NMOS dynamic and static memories. Dynamic RAMs are all routinely subjected to:

- 100% temp cycle (10 cycles, -55/150°C)
- 100% pre-burn-in continuity test (V_{CC} to ground at 25°C)
- 100% burn in at 125°C (8 hours at up to 50% overvoltage, 32 hours at nominal voltage)
- 100% functional, DC and AC parameters at 25°C
- 100% functional, DC and AC parameters at 70°C

The parts cannot be tested at 100°C.

This gives a predicted failure rate of 0.025%/1000 hours. For static RAMs whose reliability is much better (0.013%/1000 hours), burn in and temperature cycling are not used. Manufacturer (2) discourages the imposition of burn in on static RAMs. Double testing would be very good for static RAMs, however, because of the lack of pre-burn-in testing.

4.2.5 Manufacturer (2) Discrete Products Division

All power transistors are made by Manufacturer (2) in the USA with no offshore production, because of the highly automated fabrication process. Normal 100% screens are:

DC parameters at -40°C, 25°C, and 125°C ambient
Safe Operating Area (SOA) power rating tests
V_{BEF} at 10 amps

Burn in is not performed and cannot be performed at Manufacturer (2). Thermal cycling can be performed for a 2¢ per part adder and is good for catching mechanical problems. They can also provide a sample test AQL of 0.1% on outgoing products, but lot charges would be entailed on small (1000 part) lots. They said they felt 100% high temperature testing is the best screen for power transistors. The escape rate at power transistor final test is 0.4% when there is no AQL control, but by imposing AQL control the escape rate can be reduced to 0.1%.

Manufacturer (2) feels that redundant testing would be helpful. For example, when a 0.4% AQL is imposed, 15% of all lots of parts fail. It is felt that this would be reduced to 5% of all lots failing if redundant testing were imposed, a 3:1 improvement. The cost adder for redundant testing would be about 5%.

The small signal TO-92 transistors are all manufactured offshore. This raises a problem with imposing 100% DC parameter measurement at high temperature, because currently only a hot rail continuity test is performed at high temperature. Manufacturer (2) feels that full DC parameters should only be measured at 25°C; at 100°C the test should only include limited parameters.

TO-92 burn in cannot be performed by Manufacturer (2). They have no small signal transistor burn-in facilities. Temperature cycling from -65 to 150°C can be performed for a 3% to 5% cost adder and would be effective in catching intermittent opens.

4.2.6 Manufacturer (2) Bipolar Products Division

Low power Schottky (LSTTL) parts use the in-house reliability process screening when requested. Additional testing suggested by Manufacturer (2) as helpful would be ac parameters at 25°C. This would have to be performed in the U.S., however, implying special handling charges, since all in-house screen testing is done off-shore. Temperature cycling could be done over a wide temperature range of -25°C to +150°C, but would also cause special handling costs. The QRA engineering manager indicated that the thermal cycling performed with the in-house screen program (10 cycles, 0°C to 100°C) is actually water to water, but this was later disputed by the linear product marketer, who insisted that temp cycling was air to air. Water to water would be very dangerous from a reliability standpoint, according to Manufacturer (1) test results. Manufacturer (2) feels that redundant testing would be very effective in catching defects. The escape rate of 0.1% to 0.2% at final test could be reduced to 0.05% by redundant testing. Cost adders will have to be obtained through the Seattle sales office.

Reliability screening for linear microcircuits using the in-house screen program is available. The full in-house screen program costs 10¢ per part for linears and is currently performed in the USA but will soon be moved offshore.

Because of the way that the temperature cycling is performed, a wider temperature range could not be accommodated, but a larger number of cycles could be. Redundant testing could be performed as follows:

Continuity test only at 70°C: 5¢ per part adder
DC parameters at 25°C: 5¢ to 7¢ per part adder

4.2.7 Manufacturer (3)

The Manufacturer (3) in-house screen program provides a degree of reliability assurance and is similar to the in-house screen programs of other manufacturers. The program has not been used for their NMOS products but there was no objection to providing the program for NMOS products. Manufacturer (3) feels that temperature cycling is not a very effective screen, but is willing to perform extended numbers of cycles (say 30) as opposed to changing the range of temperature to greater than their 0/100°C air-to-air range. Manufacturer (3) feels that it would be very costly to go to a different temperature range because it would entail changing their standard operations overseas.

For pre-burn-in tests, Manufacturer (3) recommends that 25°C functional and DC parameters be used but that 100°C testing would not be necessary.

For burn in Manufacturer (3) often uses 40 hours at 150°C rather than 168 hours at 125°C, based on an activation energy of 1.0ev. For certain high voltage devices, they recommend that the burn in be limited to no more than 48 hours. The feeling is that 95% of the early failures are caught by this time and longer burn in will result in the migration of contaminants which will shorten the useful life.

Overvoltage testing is felt to be very useful for CMOS parts as a screen for oxide defects. Manufacturer (3) performs CMOS overvoltage testing at wafer probe on a 100% basis and would be willing to add this test at final electrical test as a 100% screen for the NASA reliability flow.

For post-burn-in electrical test, Manufacturer (3) could live with a 2% PDA. They also indicated that the current practice of only functional tests at 100°C could be extended to functional and DC parameters at 100°C if the electrical limits were widened at the 100°C temperature. Redundant or double testing could be added easily.

The cost adders for performing the in-house screen program or the augmented NASA flow testing would have to be obtained by written request to the marketing organization through the Seattle office.

4.2.8 Manufacturer (4)

Manufacturer (4) has a reliability assurance program to perform screening on plastic encapsulated bipolar TTL products, but the program does not extend to NMOS microprocessors or memory nor to bipolar memory products. Manufacturer (4) feels that their approach is one of total commitment to reliability, and thus the in-house screen program is only a marketing gimmick. Since the business at Manufacturer (4) is extremely good and they are having difficulty keeping up with the demand for their products, marketing gimmicks are not really needed and they are unwilling to extend the in-house screen program to any other products. In addition, they are unwilling to perform any special testing over and above the in-house screen testing, such as redundant testing. It was apparent that it will be difficult to consider participation by this manufacturer in a NASA standard flow for screening of plastic encapsulated parts. This is regrettable because their devices probably would be very reliable because of the tight feedback they use to correct processing problems.

But since there would be no assurance of the actual integrity of the outgoing product, it would be necessary to trust the manufacturer completely for reliability, and this has historically proven to be a dangerous position for parts procurement, no matter how good the manufacturer claims to be.

One test that Manufacturer (4) uses would be considered very undesirable. This is thermal cycling which, in their case, is a water-to-water thermal shock. It is felt that this is quite dangerous, since tests by Manufacturer (1) have shown that such an approach caused serious problems after 10,000 hours of life testing. Even though Manufacturer (4) claims they have no problems, it is felt that water-to-water should be avoided in all cases.

4.2.9 Manufacturer (5)

Manufacturer (5) has available a reliability assurance program for screening plastic encapsulated microcircuits.

Manufacturer (5) is willing to be very flexible in performing special screens that may be desirable for NASA parts. In fact, surprisingly, Manufacturer (5) suggested that two effective screens would be to perform precap visual and x-ray inspection of all parts; these tests were previously been felt to be very expensive to perform on a commercial plastic part and have been avoided in previous discussions.

The in-house reliability screening is all performed onshore, but sometime in the future this may be moved offshore. Because of the onshore testing, the performance of special tests is easy to implement.

The temperature cycling performed by Manufacturer (5) is 0/100°C liquid to liquid (nonwater). For this reason it would be difficult to go to a wider temperature range, but they would be willing to go to a larger number of cycles such as 30.

Pre-burn-in testing consists of 25°C functional and DC parameters measured for the purpose of making class sorts. Burn in is generally 125°C for 168 hours, but sometimes 150°C for 80 hours is used. Post-burn-in testing could easily be performed twice (redundant tests) at both 100°C and 25°C. Manufacturer (5) would be willing to live with a 2% PDA rather than the current 10% PDA.

It was suggested that for linear devices one of the most effective screens would be measurement of delta changes in certain parameters. This would cost 50¢ per part but would be very desirable.

Overvoltage tests are not performed to any great degree by Manufacturer (5) beyond measurement of the devices at their maximum rated voltage. Implementation of a 100% overvoltage test would require a $1500 per part type charge to cover the cost of making a new test tape.

The only transistors that are plastic encapsulated are quad arrays. They recommend that the JANTX devices be used instead of plastic transistors since the cost of the hermetic JANTX parts is very low. This should be verified by an actual cost comparison.

Preparation of a budgetary cost estimate to cover the proposed NASA standard flow will have to be coordinated through the Seattle representative. The current cost adder for performing the in-house screen program ranges from 15¢ to $1.00 depending on the product type and complexity.

4.2.10 Manufacturer (6)

This manufacturer has run extensive reliability tests on their bipolar TTL-type products that show that in the first 1000 hours of accelerated life test there is little difference between plastic and hermetic parts but after 4000 hours there is a significant difference between the two, with plastic having twice the failure rate.

Manufacturer (6) has an in-house program for reliability screening of some of their products, with a version that calls for burn in of plastic parts. They are willing to supply the following part types screened to this version:

- TTL
- LSTTL
- STTL
- ASTTL
- Bipolar Memory
- NMOS Memory
- CMOS
- Linears

There was some question and hesitancy about providing in-house screening for the following part types:

NMOS Microprocessors
Bipolar Microprocessors

In-house screening cannot be provided at all for transistors or diodes.

For lot sizes in the range of 1000 parts such are envisioned for NASA procurements, no special testing such as redundant measurements or special temperature cycling can be performed by the commercial organization. Instead, the high reliability organization would have to perform the testing for significant additional cost. It is Manufacturer (6)'s contention that if special testing is required to achieve desired reliability goals, then NASA should use JAN Level B parts instead, because the cost would be lower. The following table shows the cost comparisons for various TTL parts, one an SSI part and the other an MSI part.

SSI (7400 type)	Basic Cost	Adder for In-House Screening	Total Cost
Commercial Temp Range Plastic	17¢	25¢	42¢
Commercial Temp Range Hermetic	19¢	25¢	44¢
Military Temp Range Hermetic	30¢	$1.00 (883B Screened)	$1.30
JAN Class B Military Qualified	$1.80	---	$1.80
Commercial Temp Range Plastic with Double Testing Added to the in-house screen			$2.00 + minimum order value of $1000 per lot
MSI (74181 type)			
Commercial Temp Range Plastic	$2.50	35¢	$2.85
Commercial Temp Range Hermetic	$3.00	35¢	$3.35
Military Temp Range Hermetic	$4.00	$1.00 (883B Screened)	$5.00
JAN Class B Military Qualified	$6.00	----	$6.00
Commercial Temp Range Plastic with Double Testing Added to the in-house screen			$8.00

It can be seen from this pricing structure that Manufacturer (6) would not want to participate in any standardized testing of plastic parts that differed from their in-house reliability testing.

4.2.11 Manufacturer (7)

This manufacturer has a policy of performing reliability demonstration tests on all new products followed by a monitoring program that ensures that the products

do not fall away from the desired failure rates. The typical failure rate number goal for Manufacturer (7) parts is 0.05%/1000 hours at 55°C with a 60% confidence level.

Normal flow for all Manufacturer (7) parts, plastic or hermetic, is as follows:

- o 100% classification tests using tight guard bands. Consists of functional and DC parametric tests at 85° to 90°C to allow for die thermal rise over 70°C.
- o Final electrical tests. Microprocessors are tested at high temperature and memory devices are guard band tested at 25°C.
- o Sample tests to a 1% AQL.

If burn in were required on a 100% basis, it would be performed after final test and then another electrical post-burn-in test would be performed. Burn in has been found by Manufacturer (7) to give a 5:1 improvement in the failure rate. They do not consider a PDA (Percent Defective Allowable) after burn in. All parts that pass are deliverable. Manufacturer (7) favors a burn in of 44 hours at 125°C.

Temperature cycling can be performed but they do not feel that it accomplishes anything and would prefer not to perform temperature cycling. A possible flow for NASA screened parts by Manufacturer (7) would be:

- Double electrical measurement at 85°C
- Dynamic burn in: 44 hours at 125°C
- Electrical measurement at 85°C
- Sample testing at a 1% AQL

The cost adder for performing this test program on a 100% basis in small lot quantity (1000 parts) would be an increment of 50% to whatever the basic part cost is.

5.0 ANALYSIS OF THE DATA

5.1 Field Use Failure Rate Data Versus Time

The data gathered from the users of plastic encapsulated semiconductors described in the preceding section were tabulated in a single listing for analysis on a year-by-year basis. This tabulation appears in Appendix D. The results of this tabulation are plotted in Figures 1 through 28. Each plot depicts the failure rate of the particular part classification as a function of time. In cases where data for hermetic parts were available these data are plotted on the same plots.

5.2 Manufacturers Projection of Failure Rate

In the course of the plant visits to the part manufacturers, a number of reliability reports were obtained that projected the expected in-service failure rates for certain parts as a function of the type of screening the parts received. Table 19 summarizes these data. It must be noted that these data items are not based on actual field failure rates but only on the results of accelerated stress testing performed by the manufacturers at their own facilities. Most manufacturers project a significant improvement in the failure rates if burn-in is performed. This improvement is on the order of 5:1.

FIGURE 1. SSI TTL LOGIC

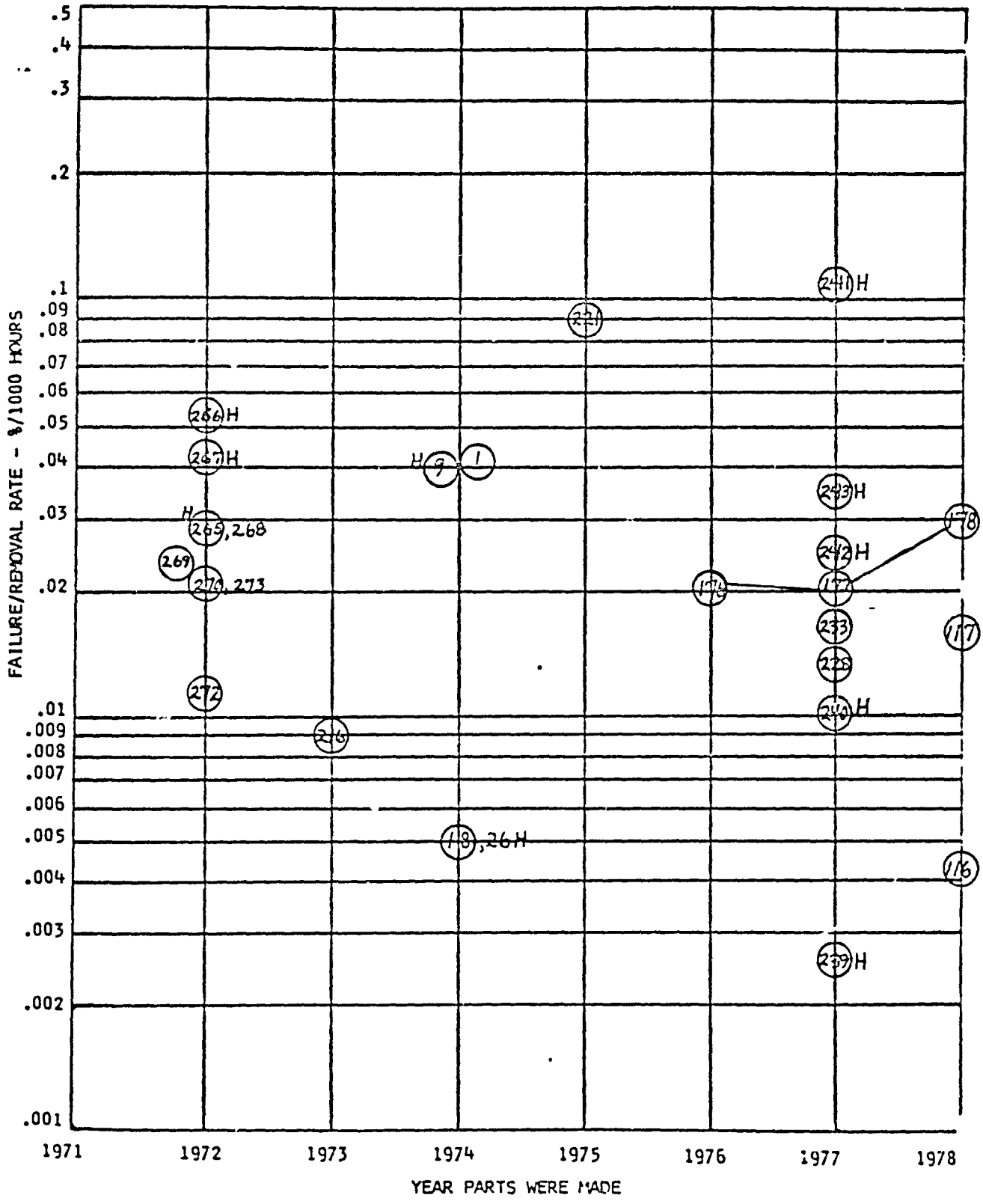


FIGURE 2. SSI LSTTL LOGIC

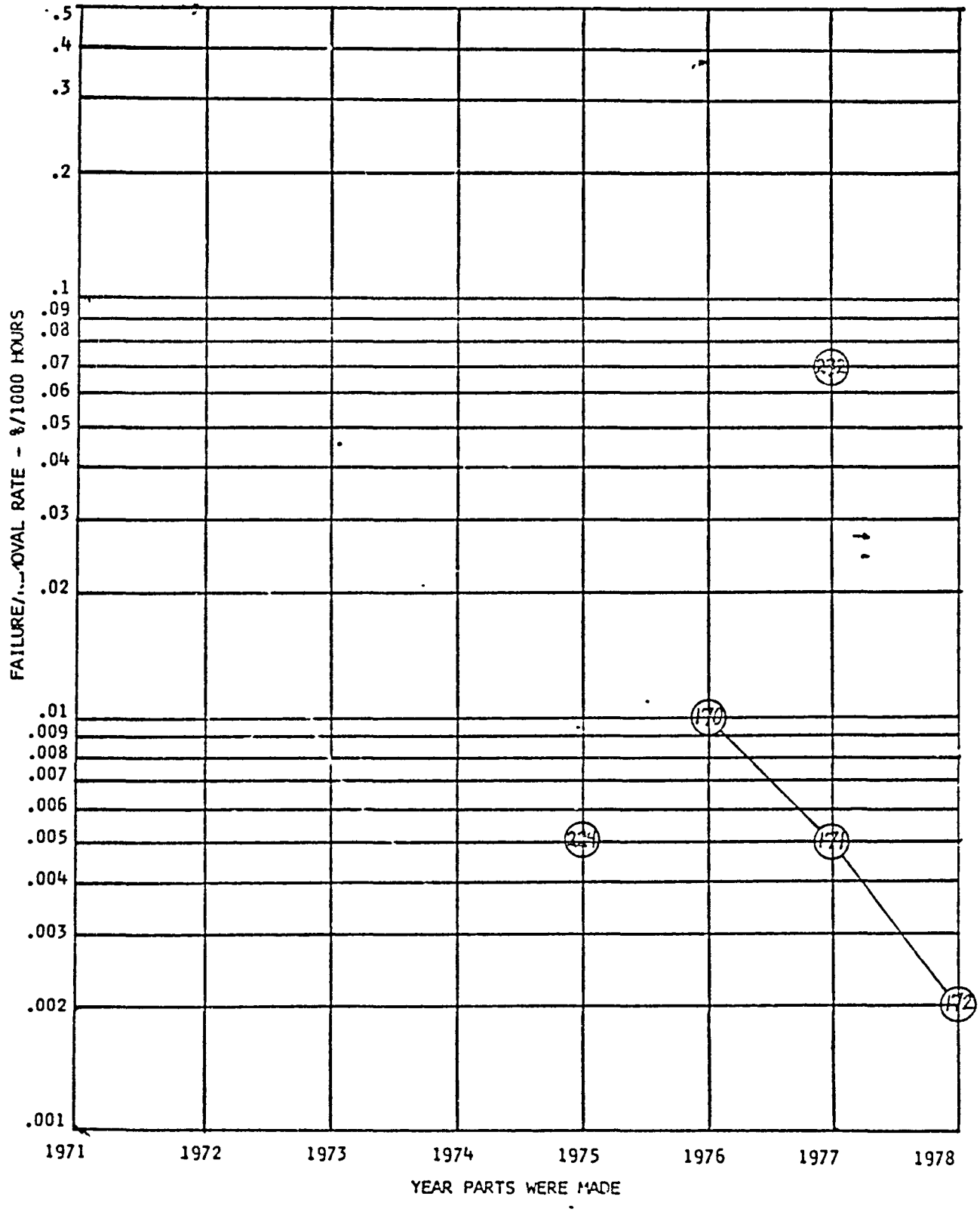


FIGURE 3. SSI STTL LOGIC

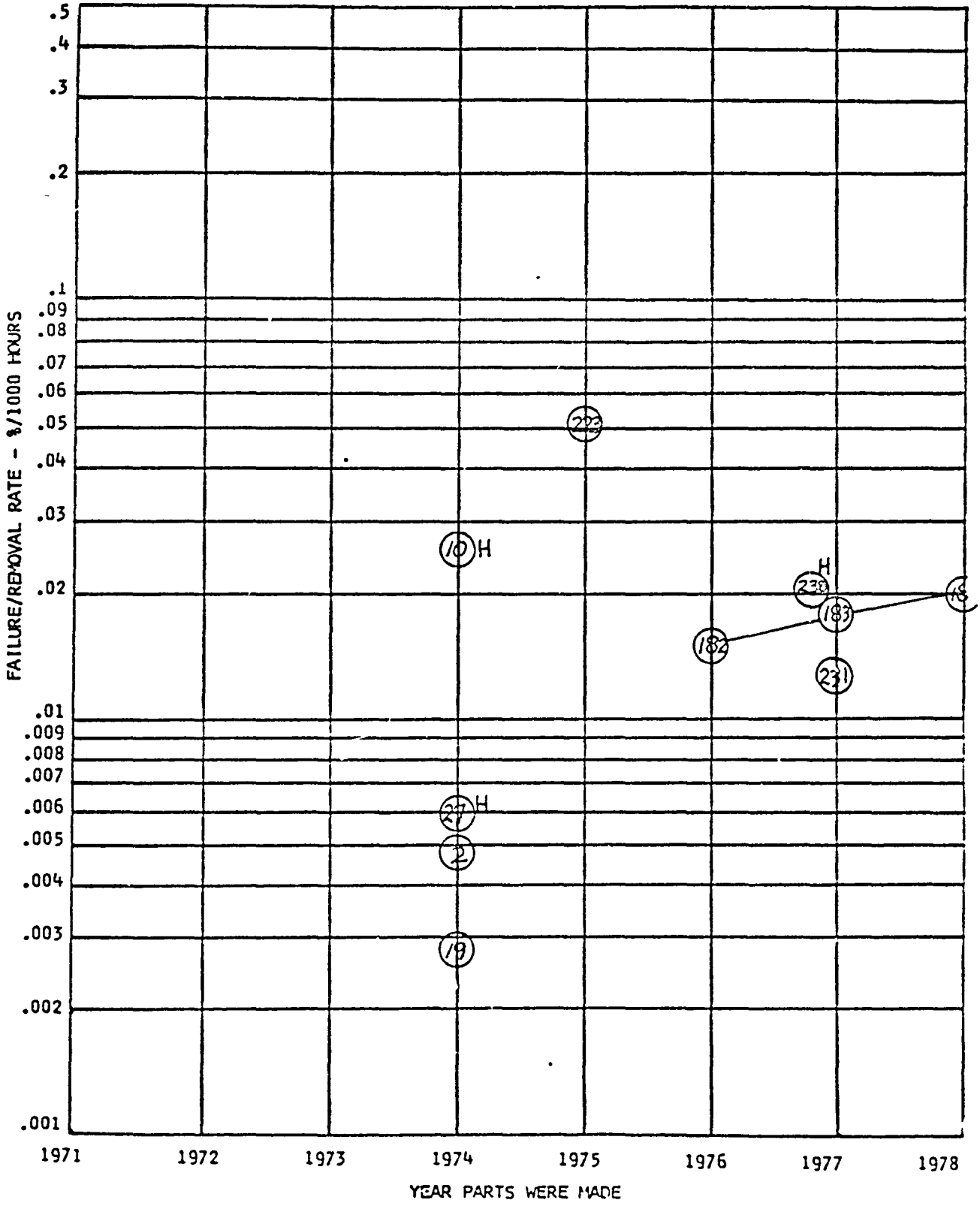


FIGURE 4. SSI HTTL LOGIC

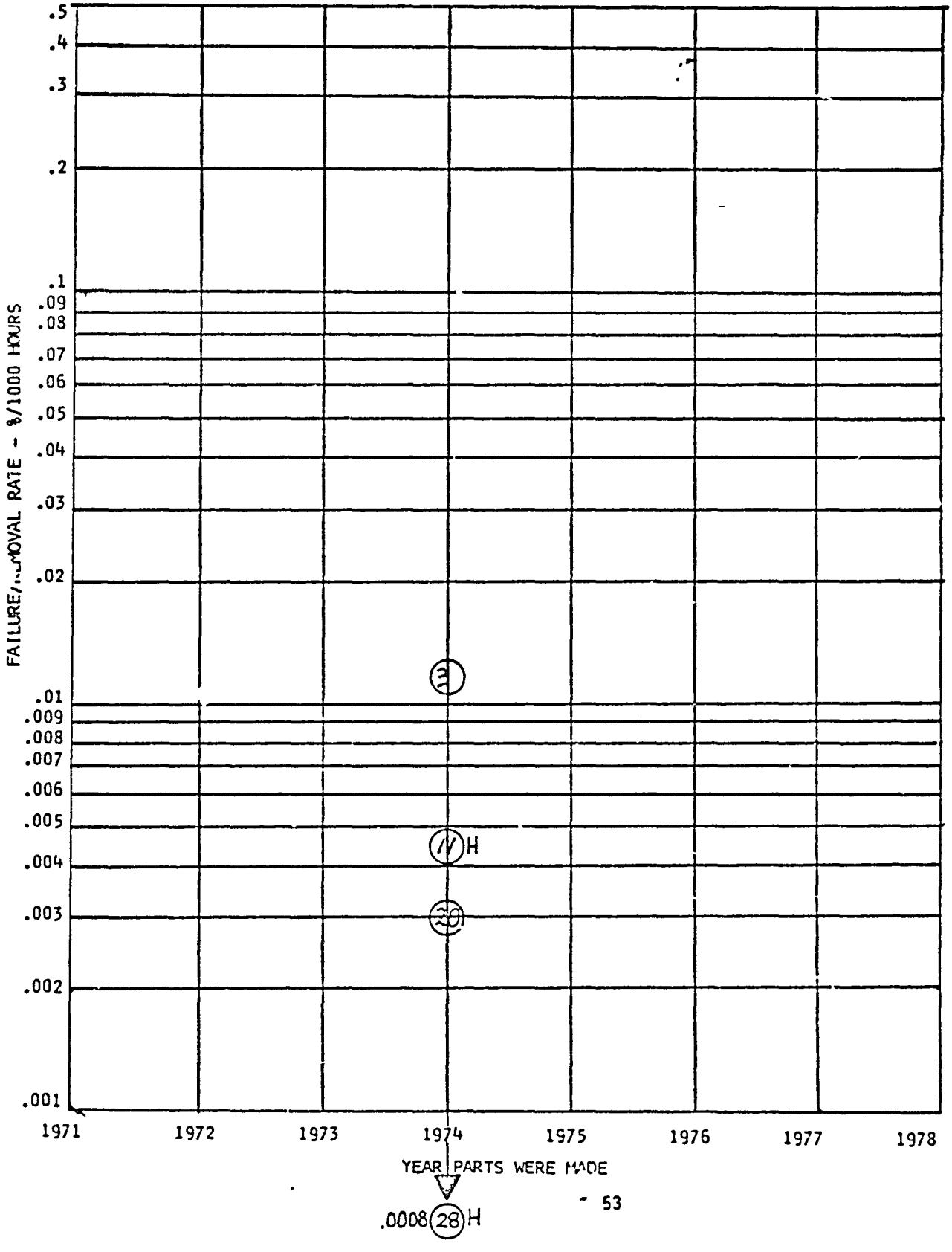


FIGURE 5. SSI ECL LOGIC

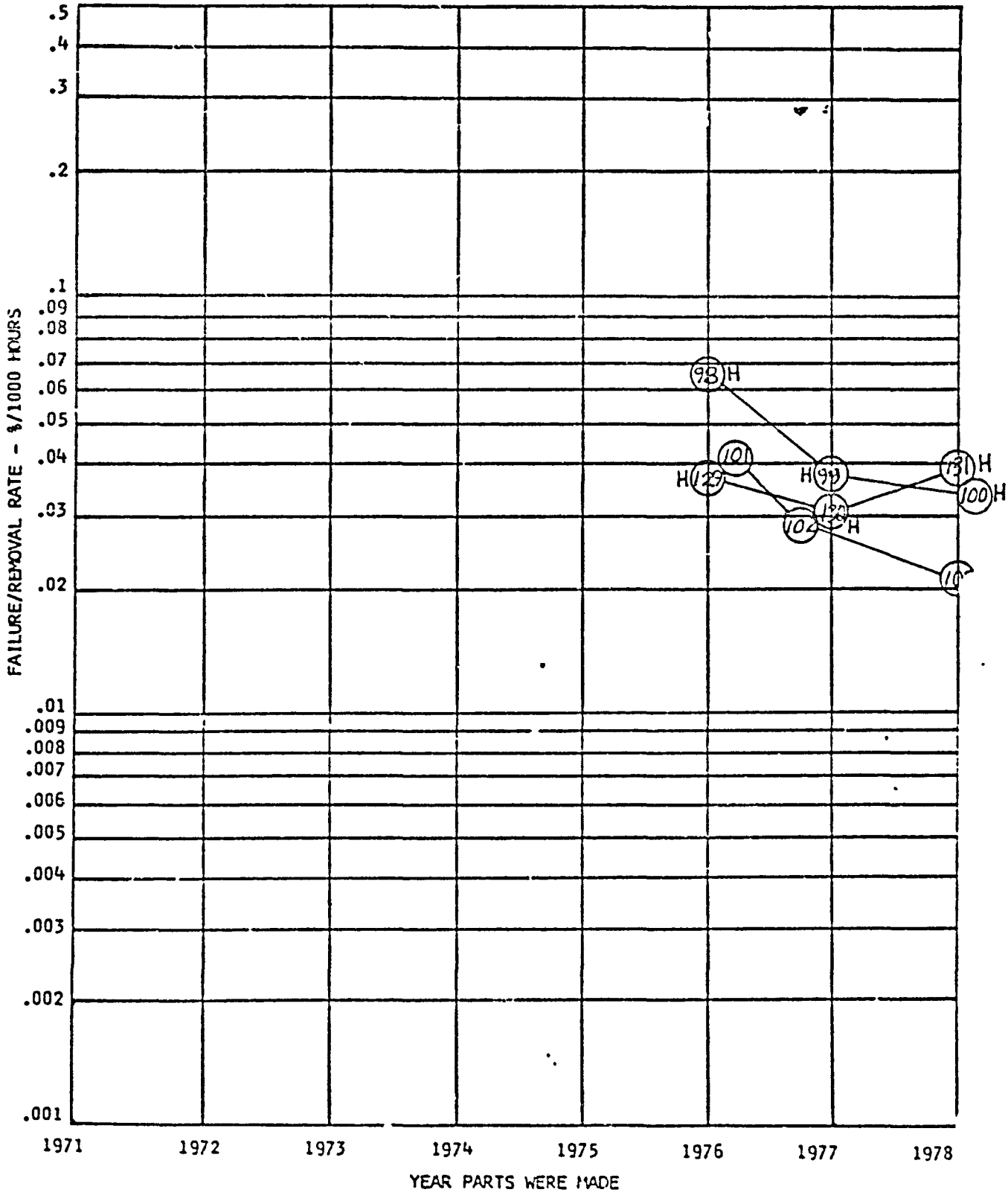


FIGURE 6. SSI LINEAR AMP

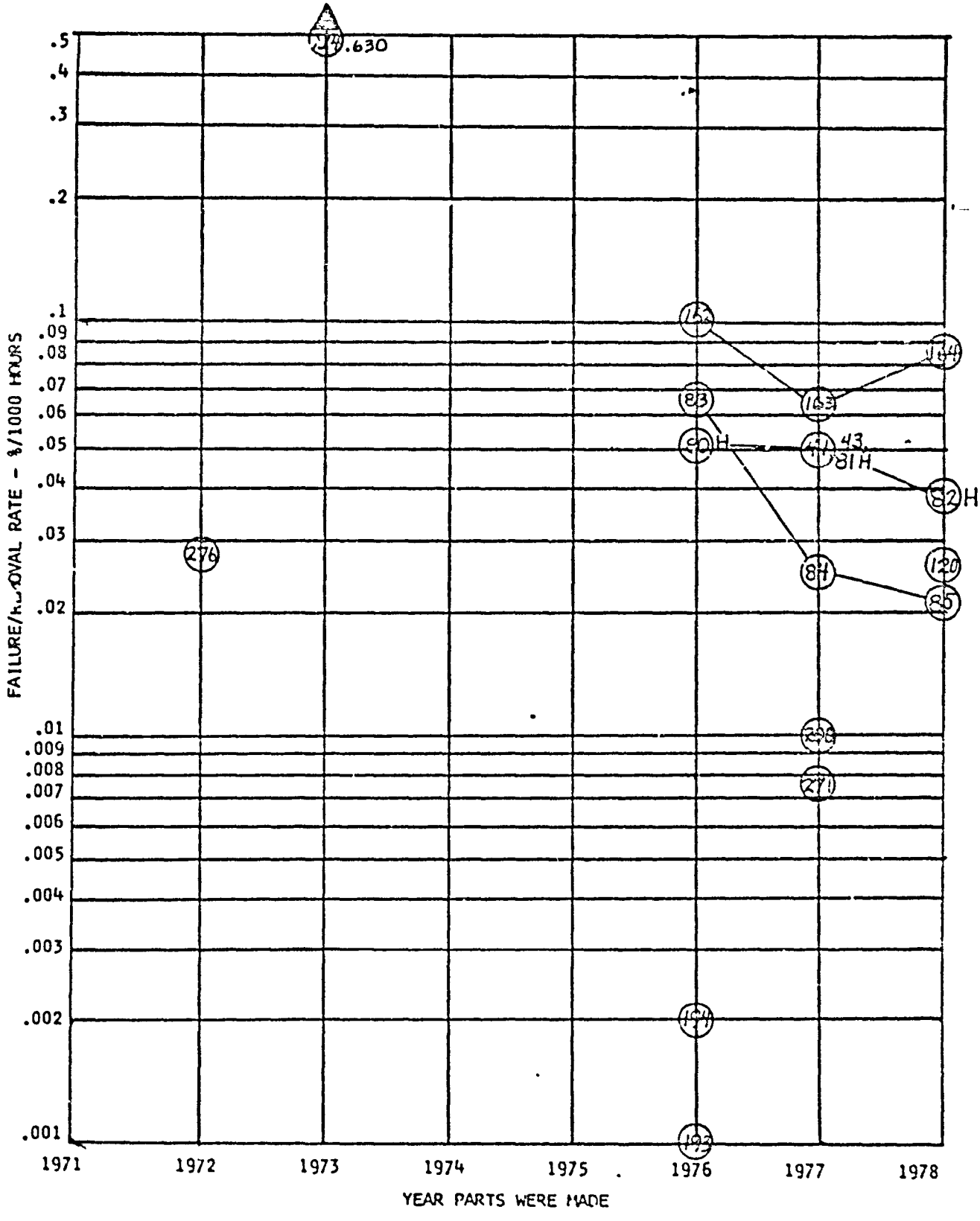


FIGURE 7. SSI LINEAR VOLTAGE REGULATOR

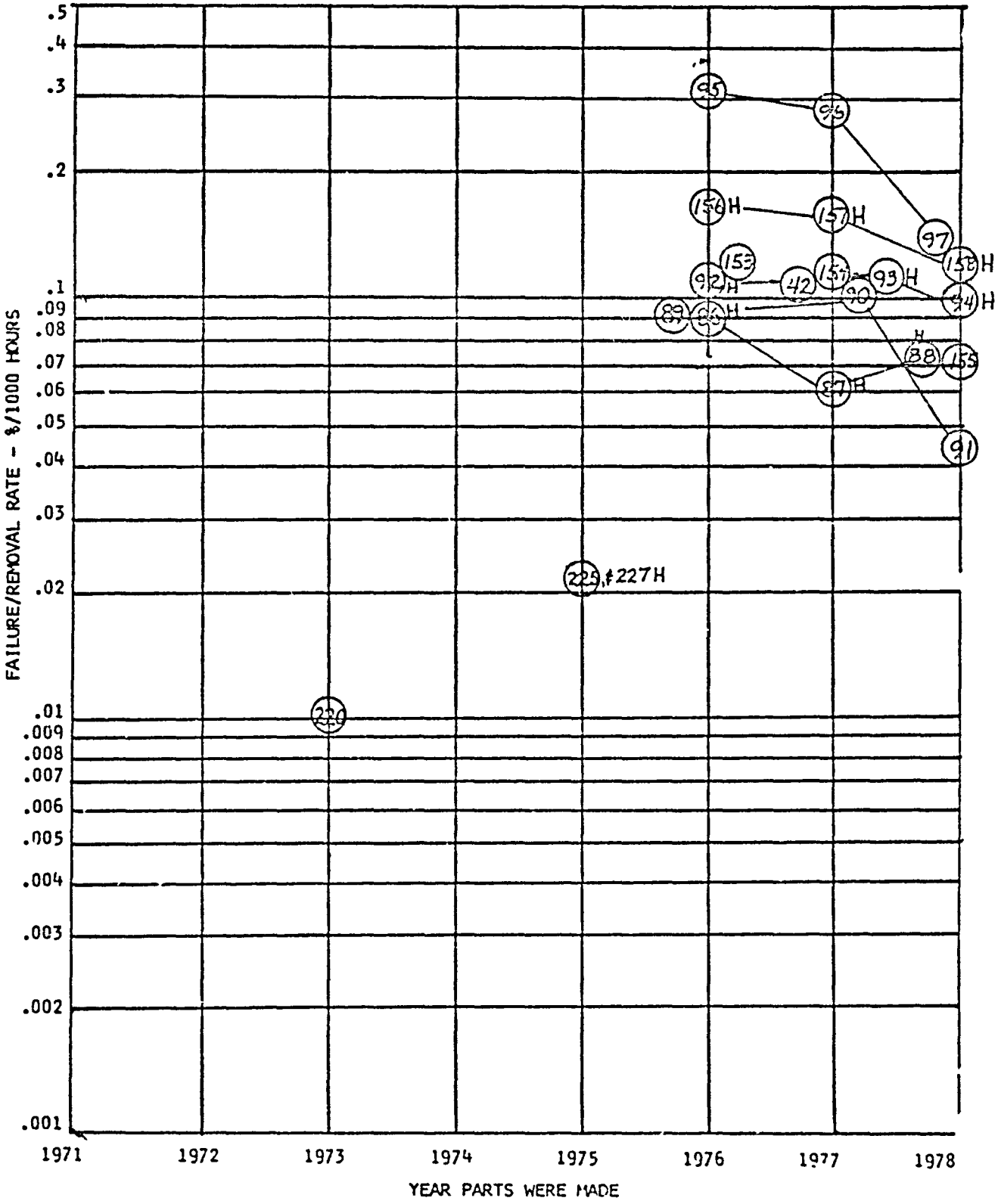


FIGURE 8. MSI TTL LOGIC

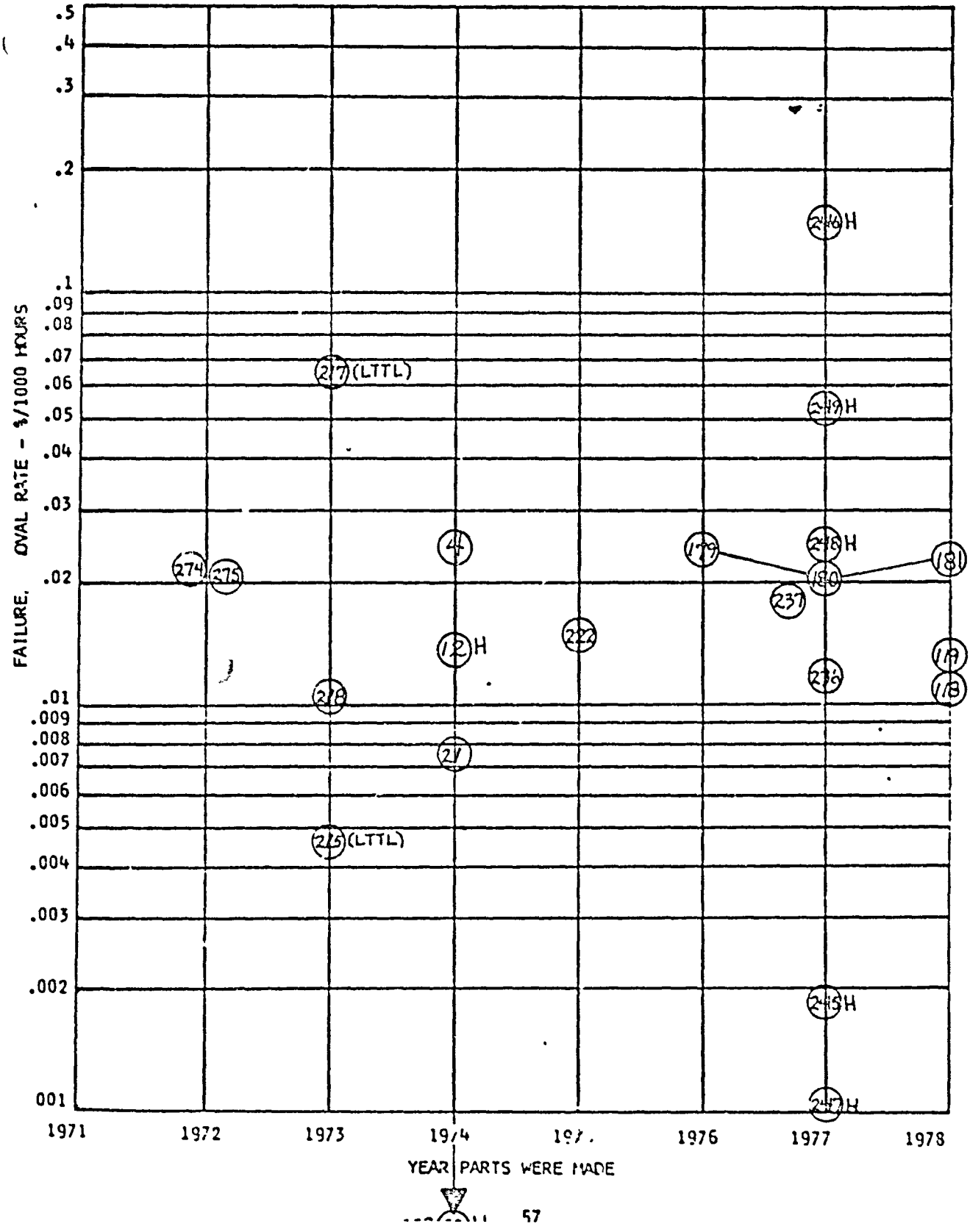


FIGURE 9. MSI LSTTL LOGIC

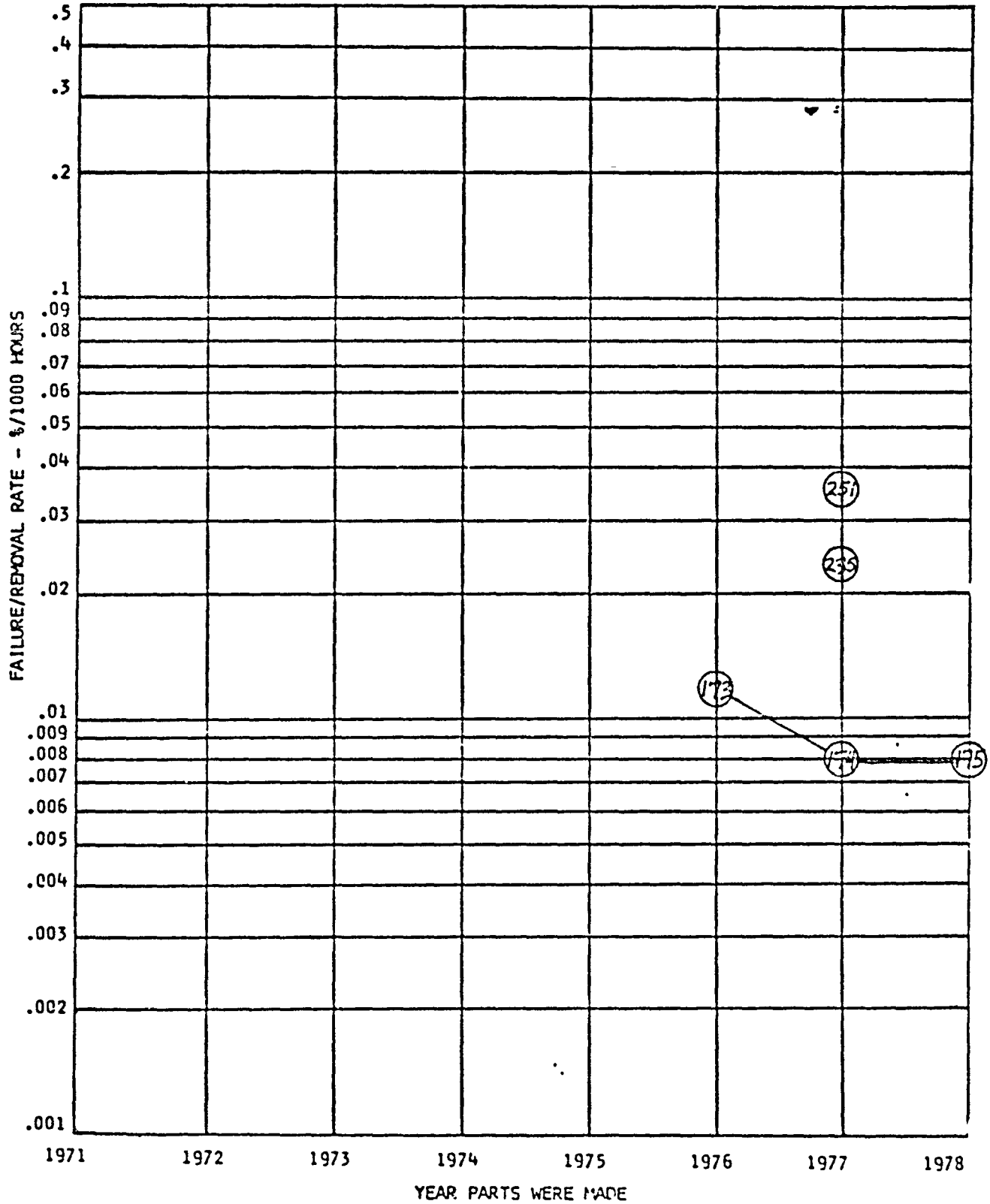


FIGURE 10. MSI STTL LOGIC/RAM

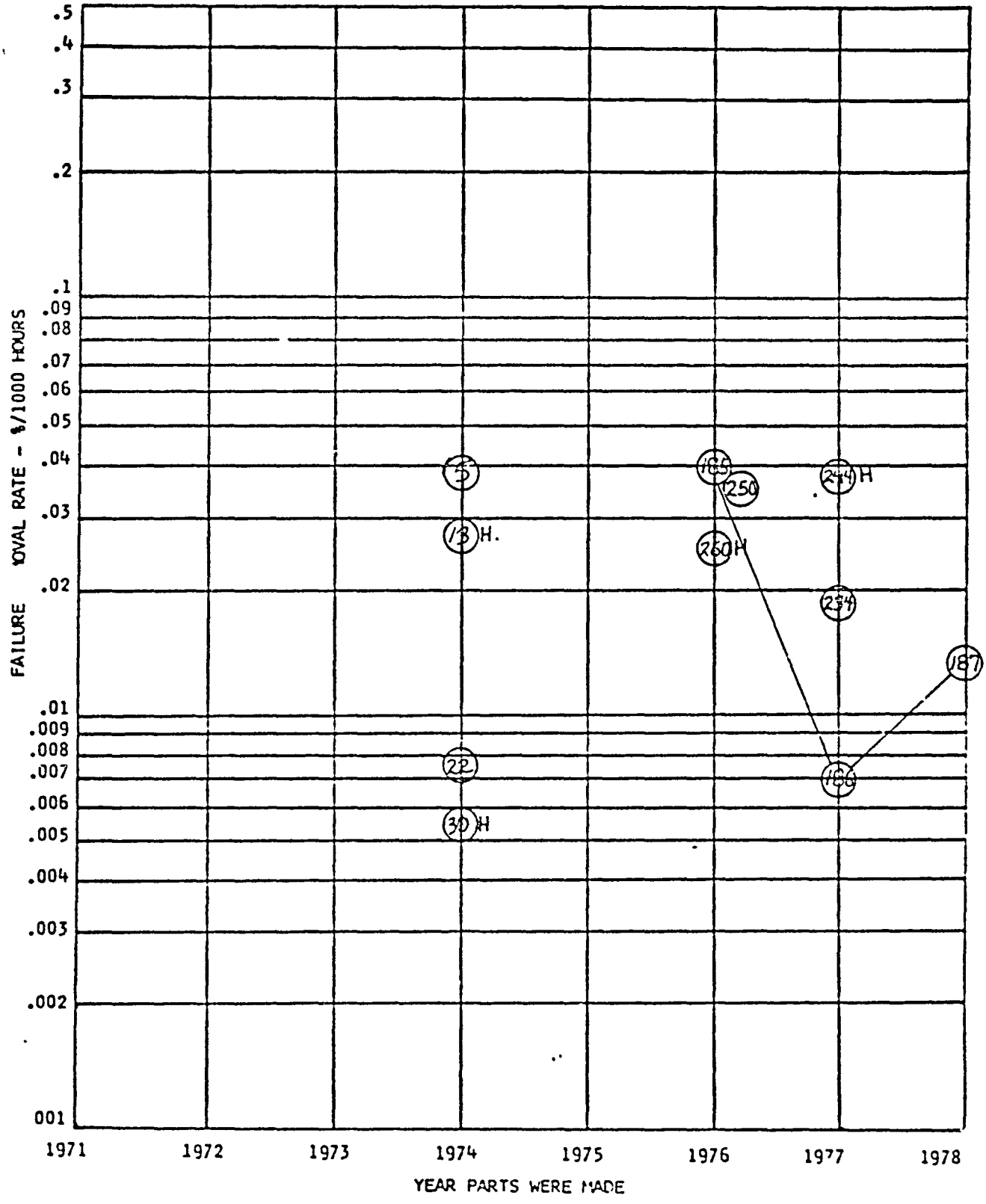


FIGURE 11. MSI HTTL LOGIC

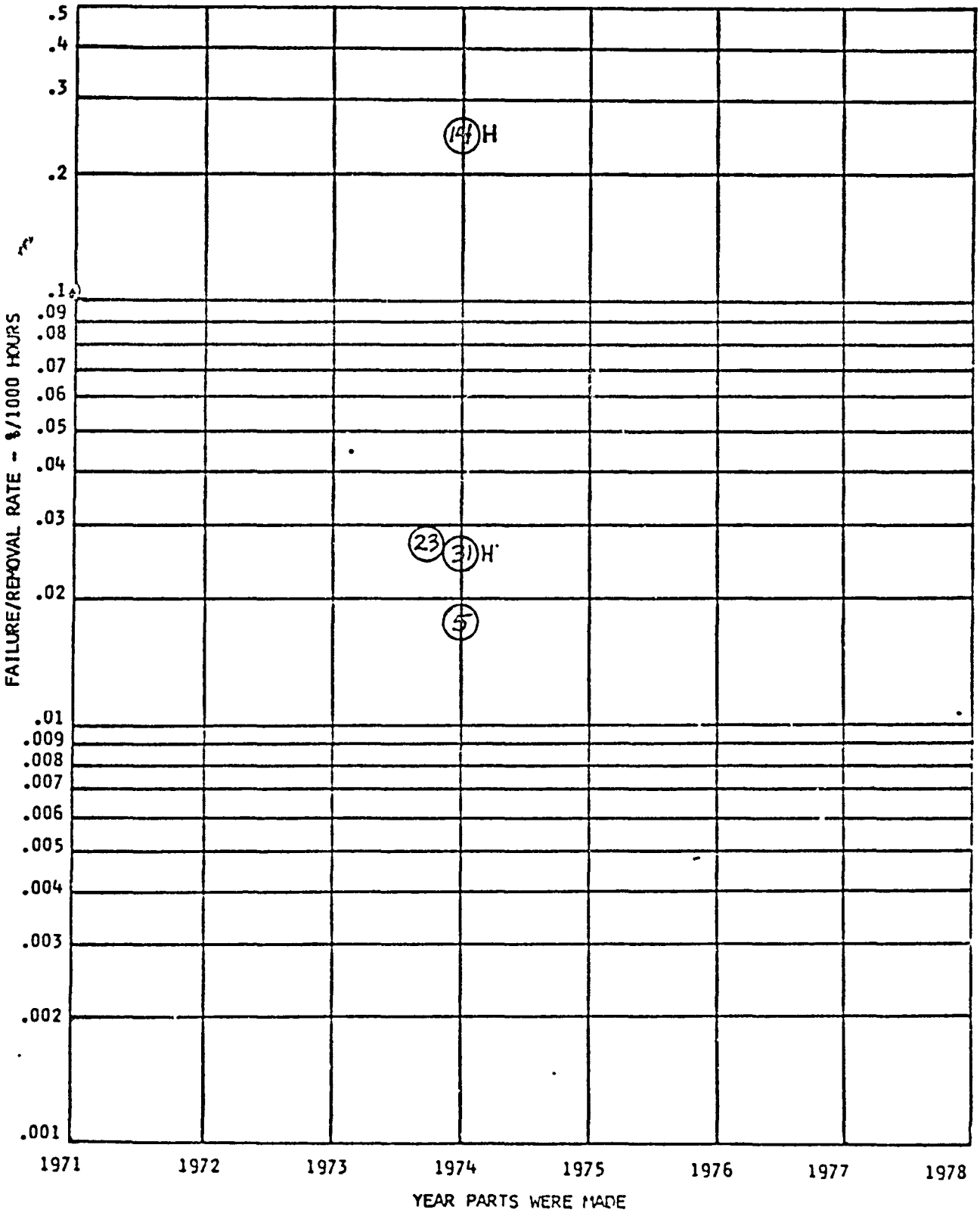


FIGURE 12. MSI ECL LOGIC

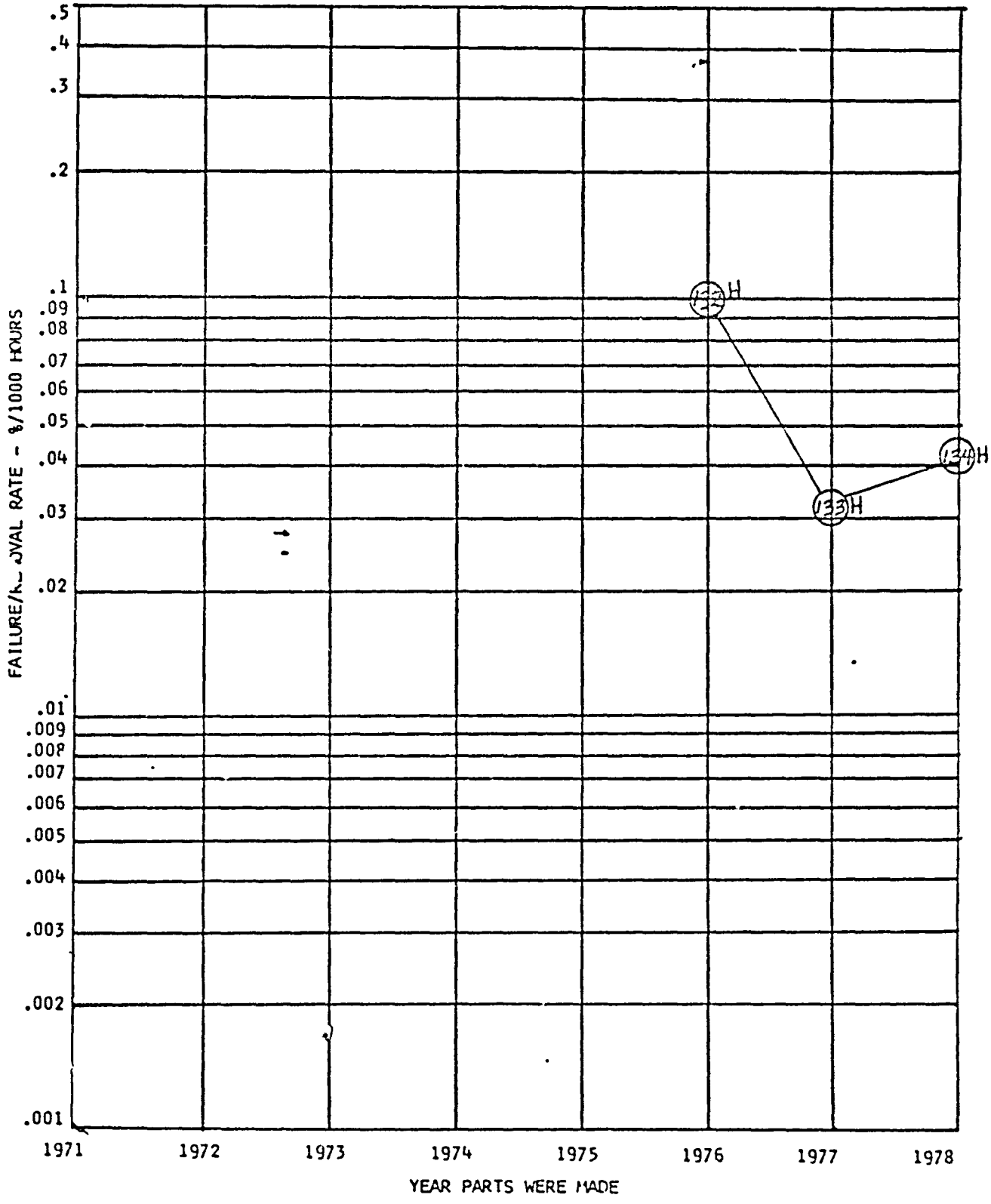


FIGURE 13. LSI RAM/LINEAR/STTL

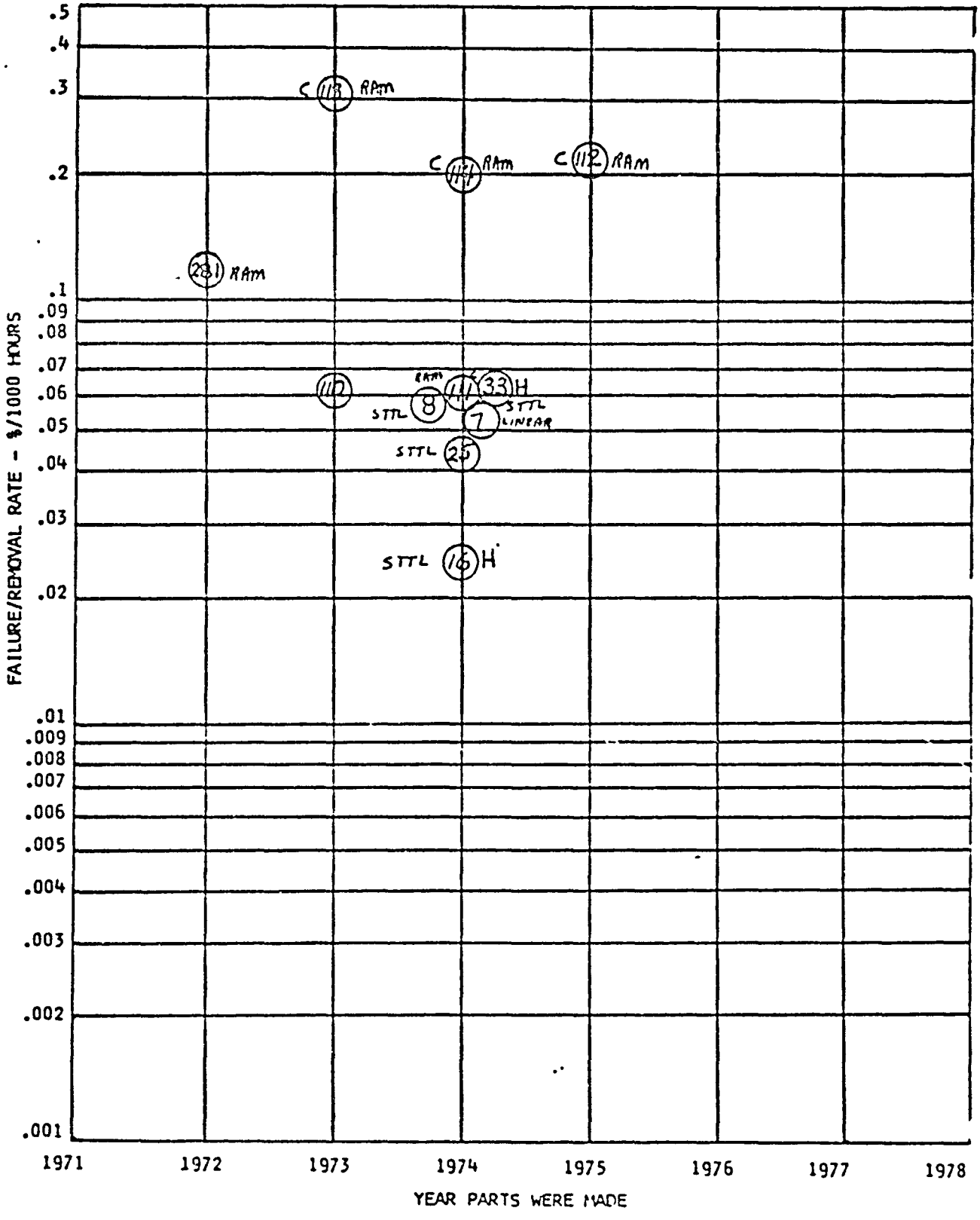


FIGURE 14. LSI ECL PROM

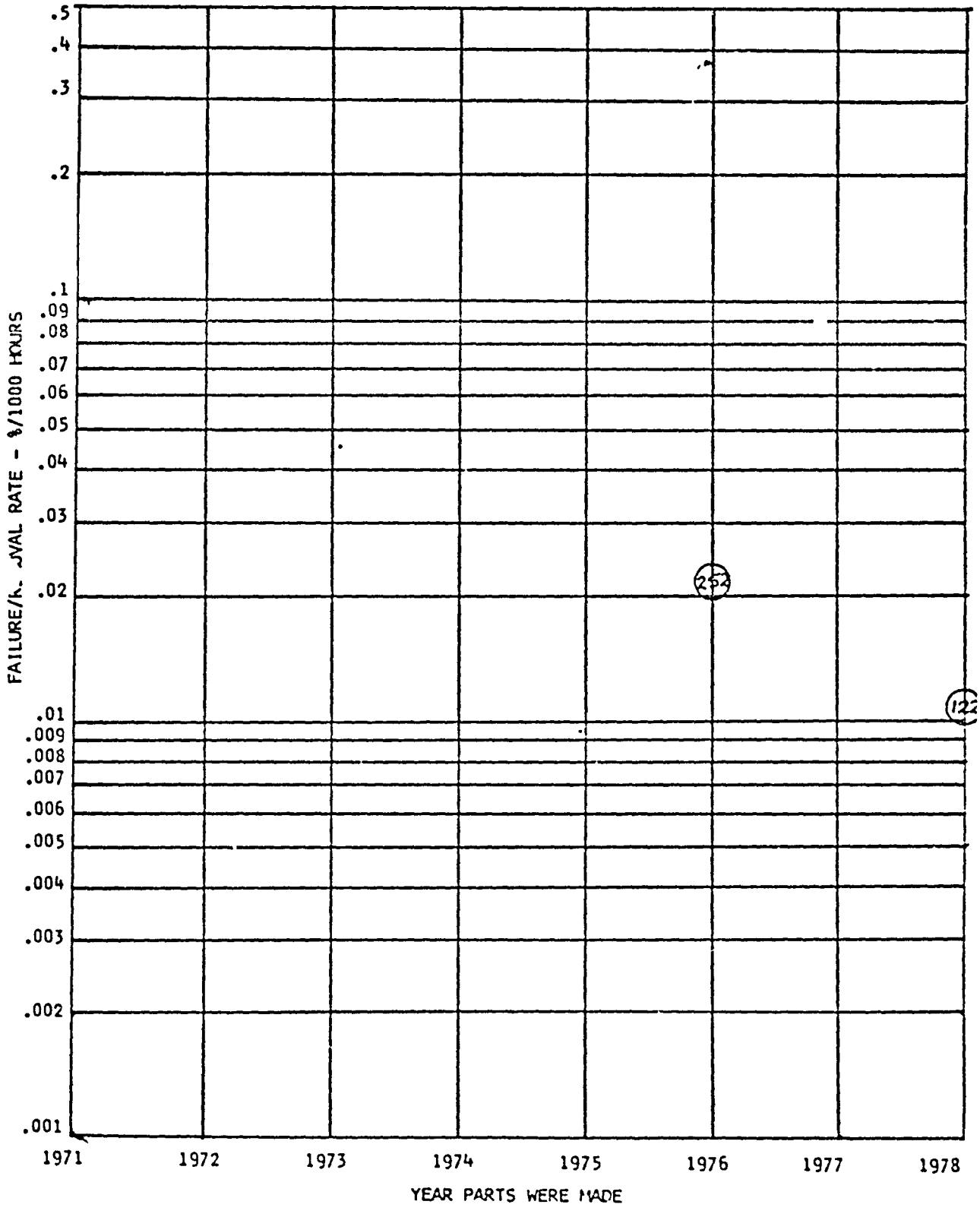


FIGURE 15. SSI CMOS LOGIC

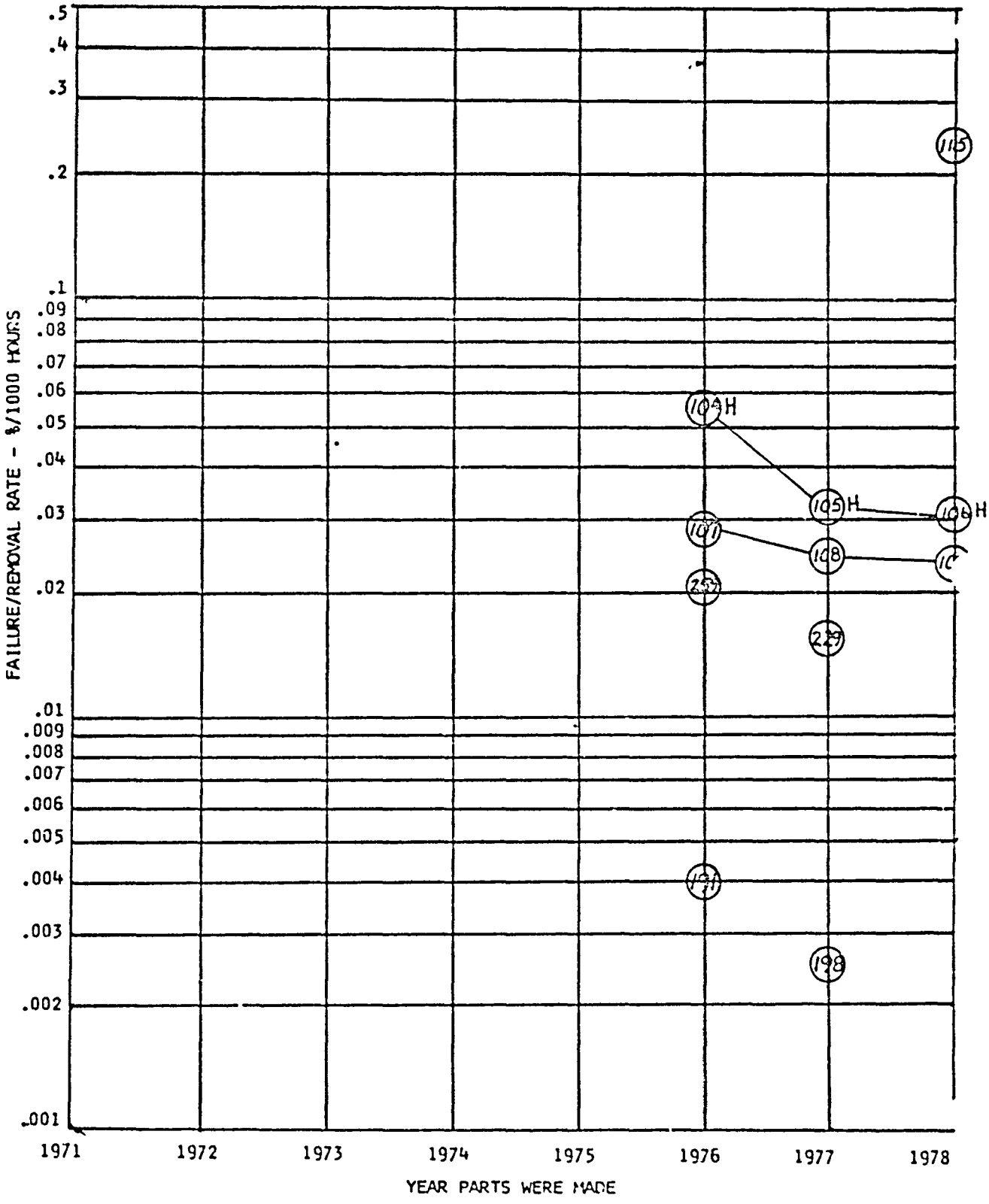


FIGURE 16. MSI PMOS LOGIC

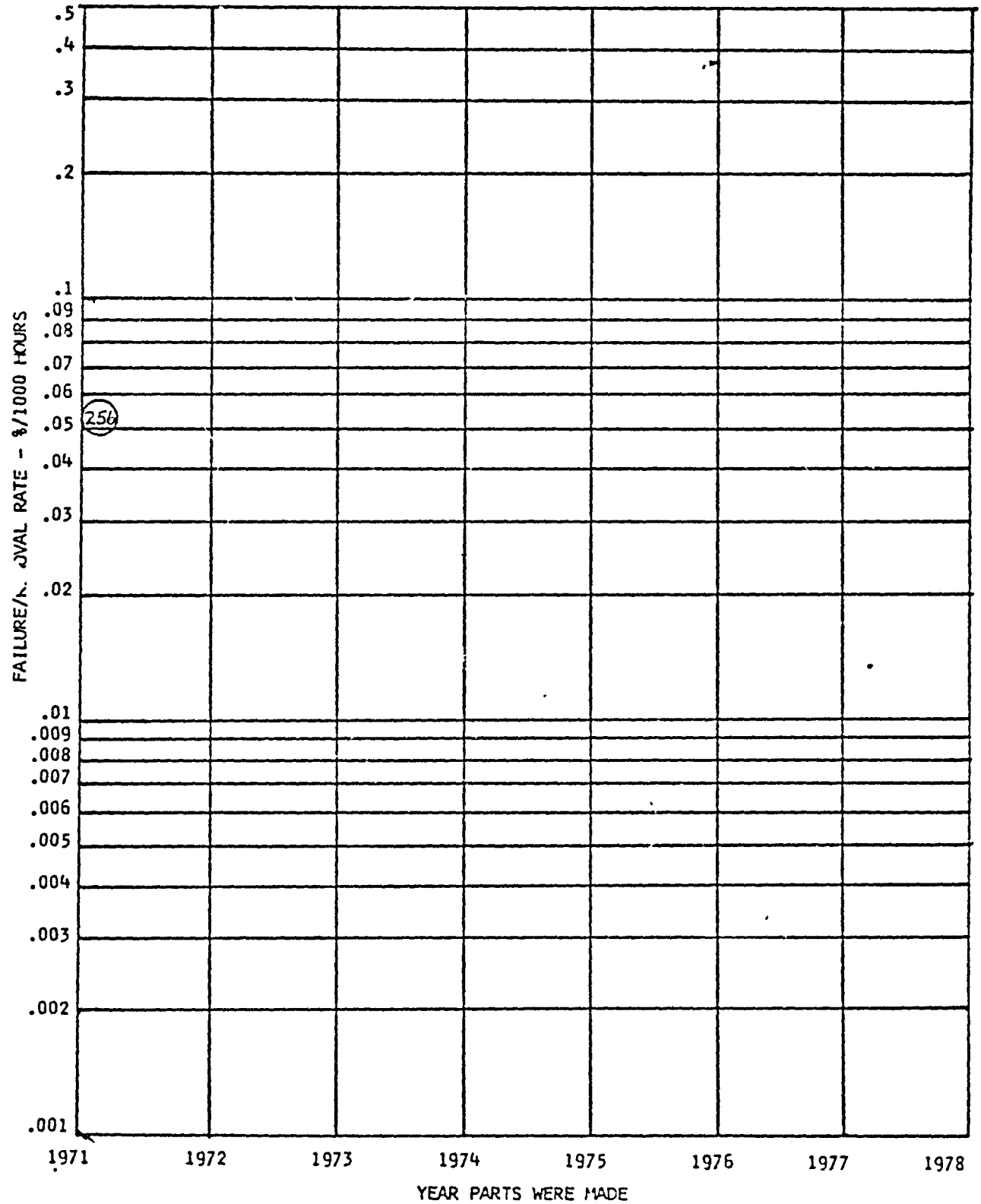


FIGURE 17. LSI NMOS MICROPROCESSOR

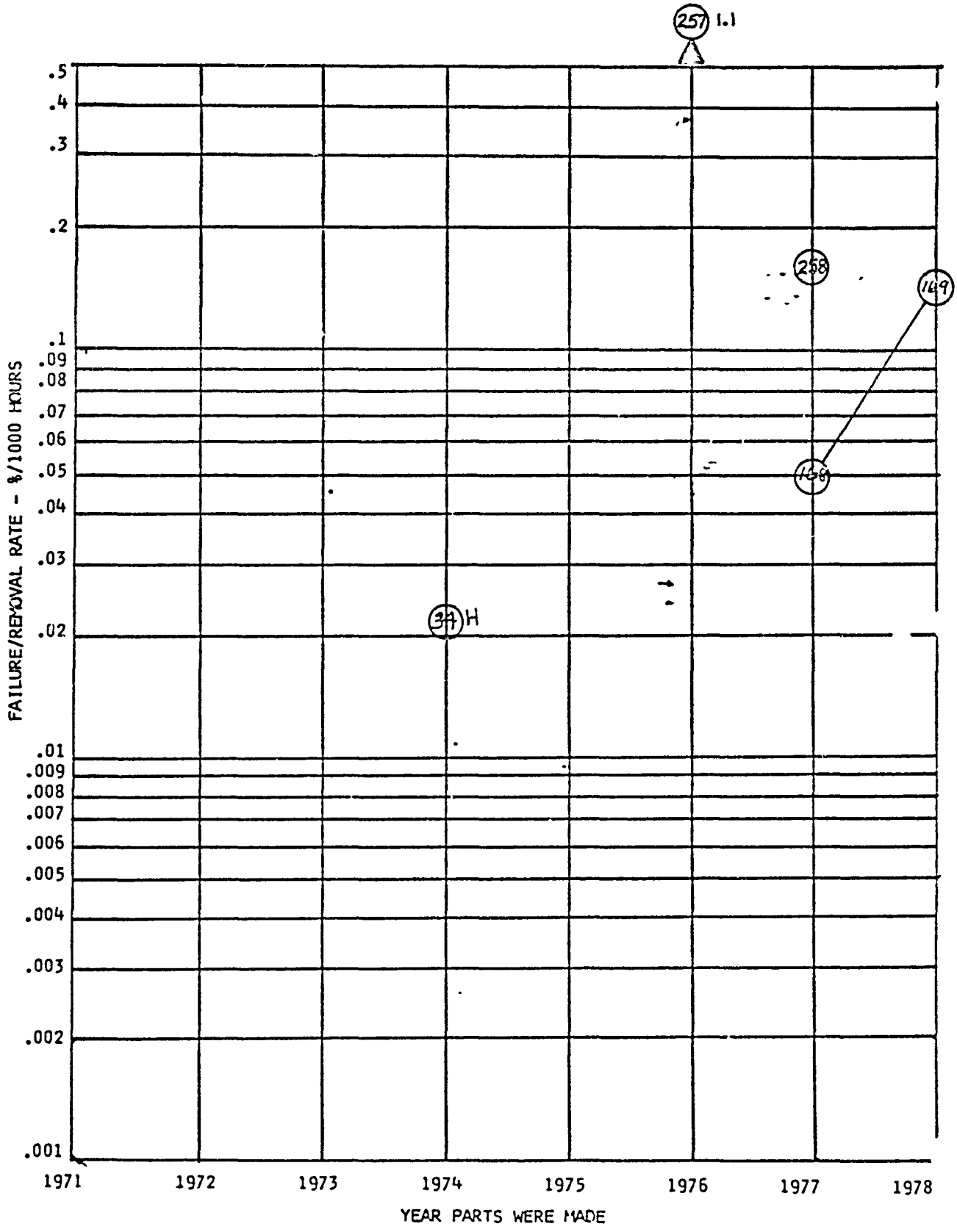


FIGURE 18. LSI NMOS RAM

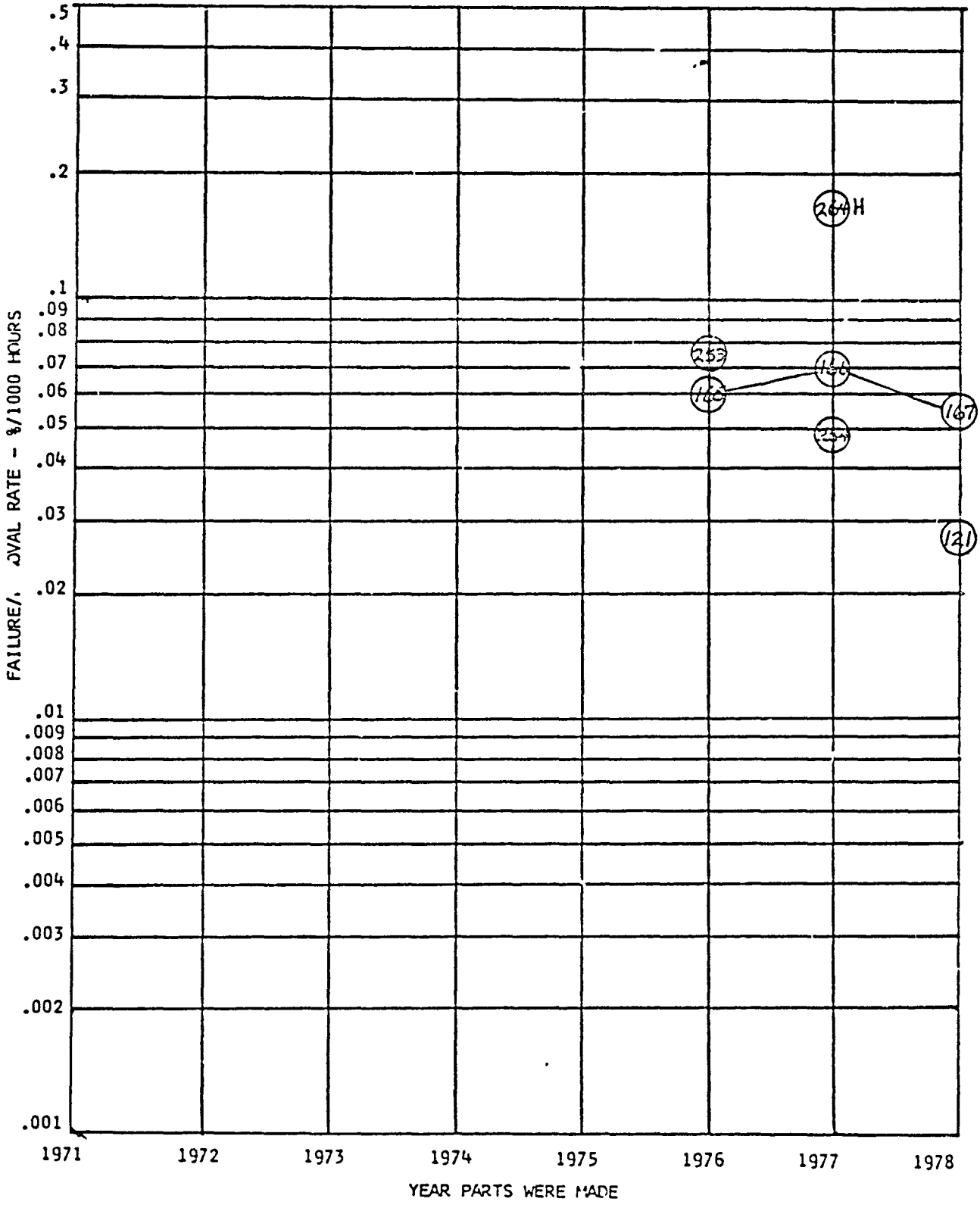


FIGURE 19. LSI PMOS LOGIC

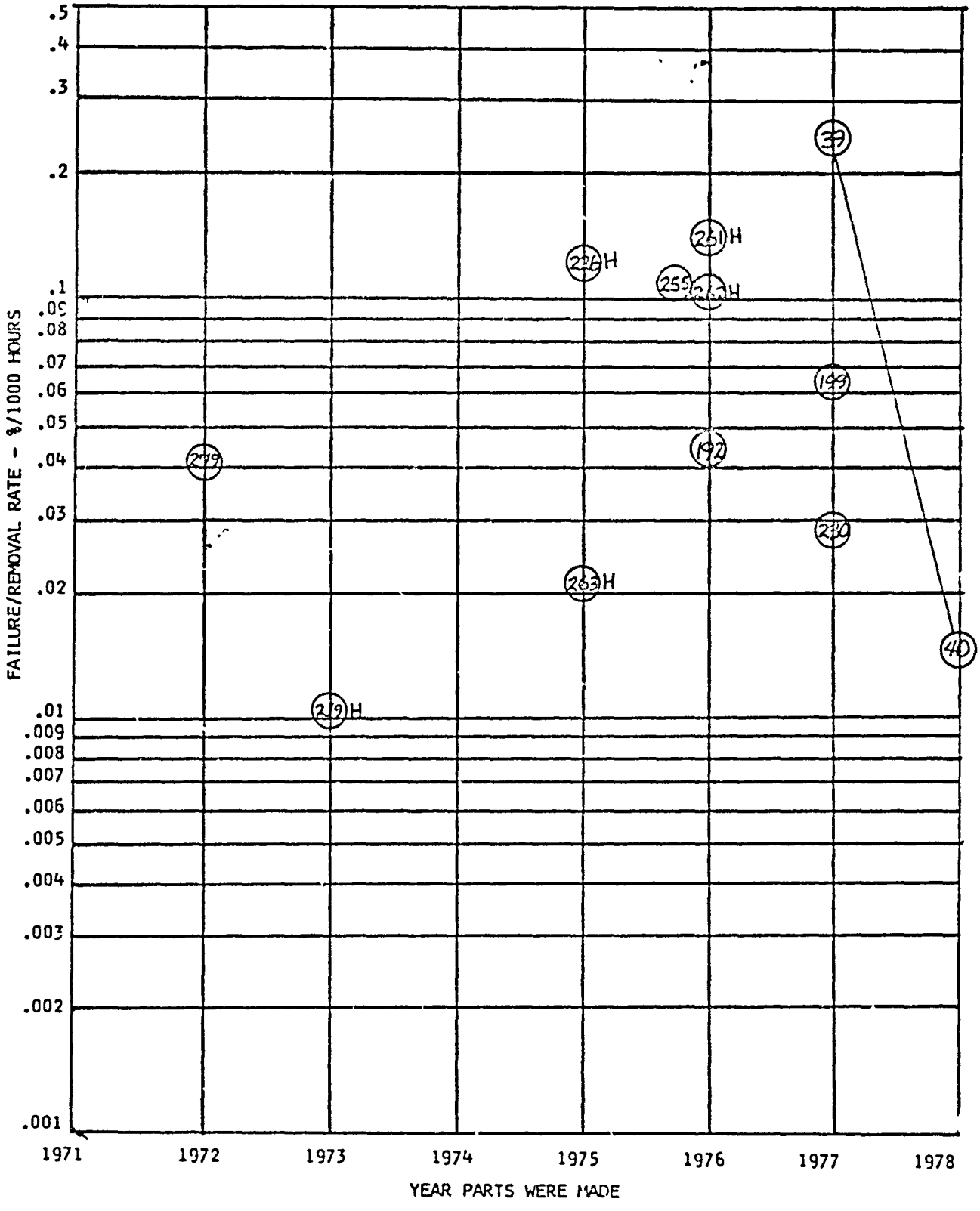


FIGURE 20. LSI PMOS RAM

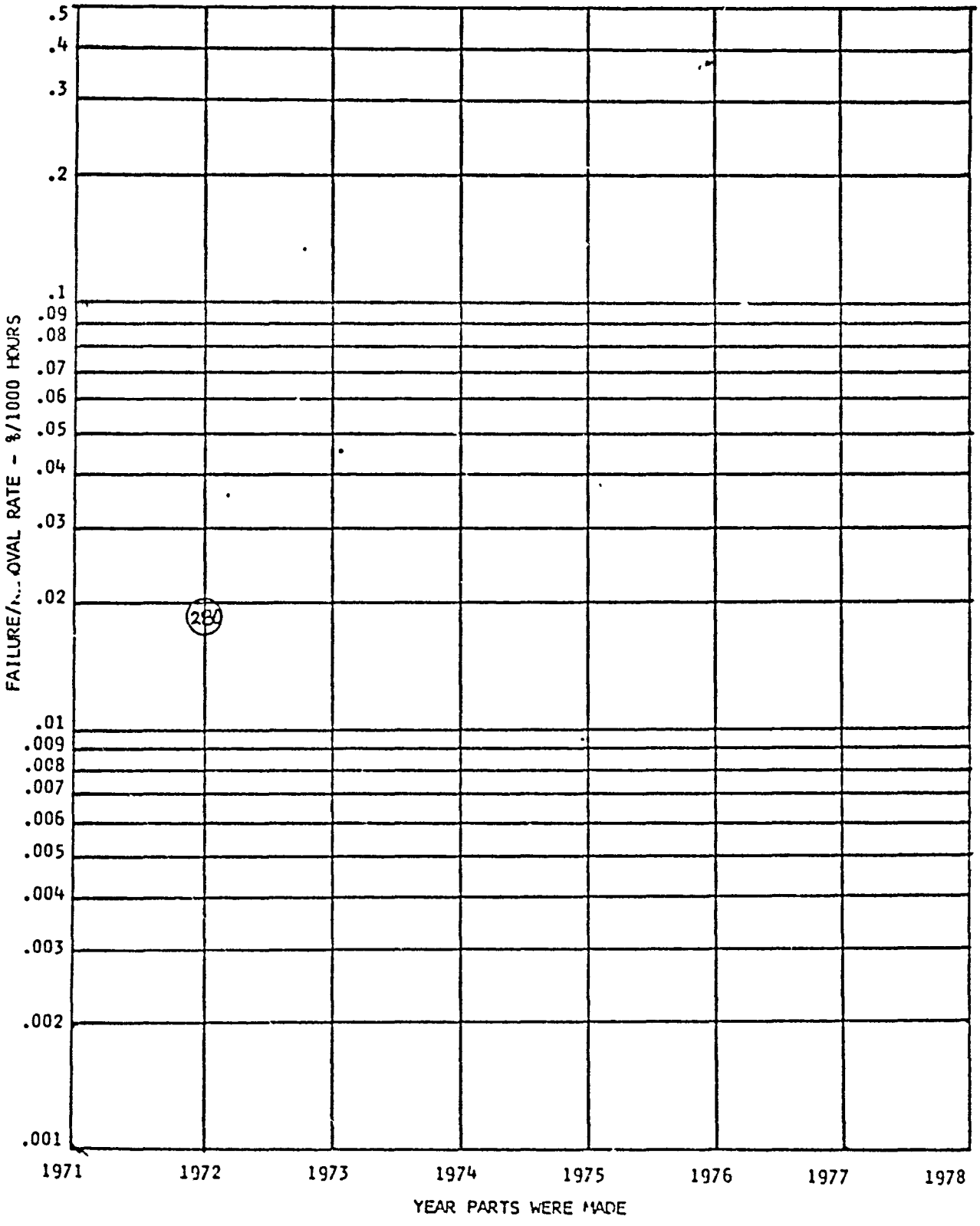


FIGURE 21. LSI PMOS ROM

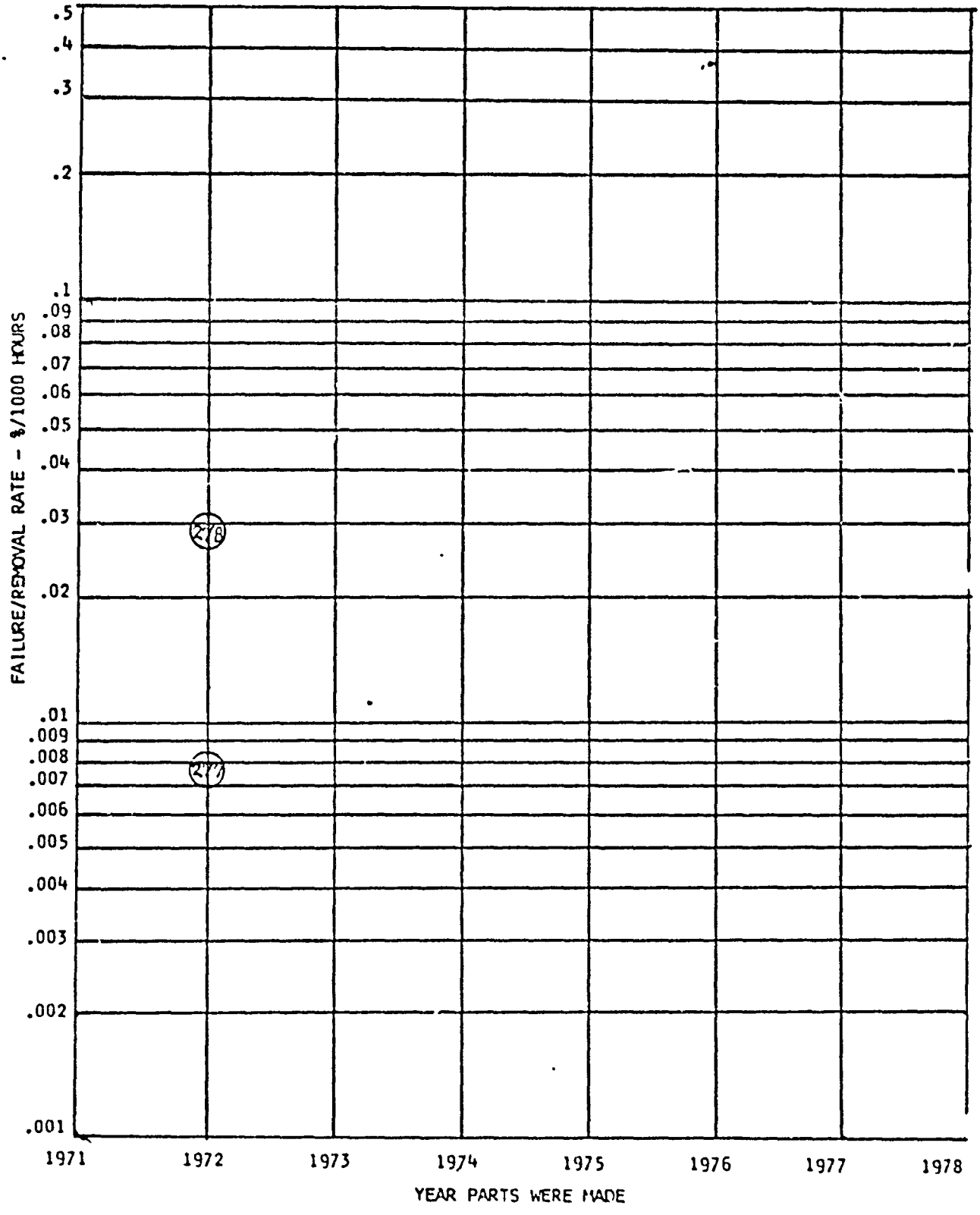


FIGURE 22. TRANSISTOR SS NPN

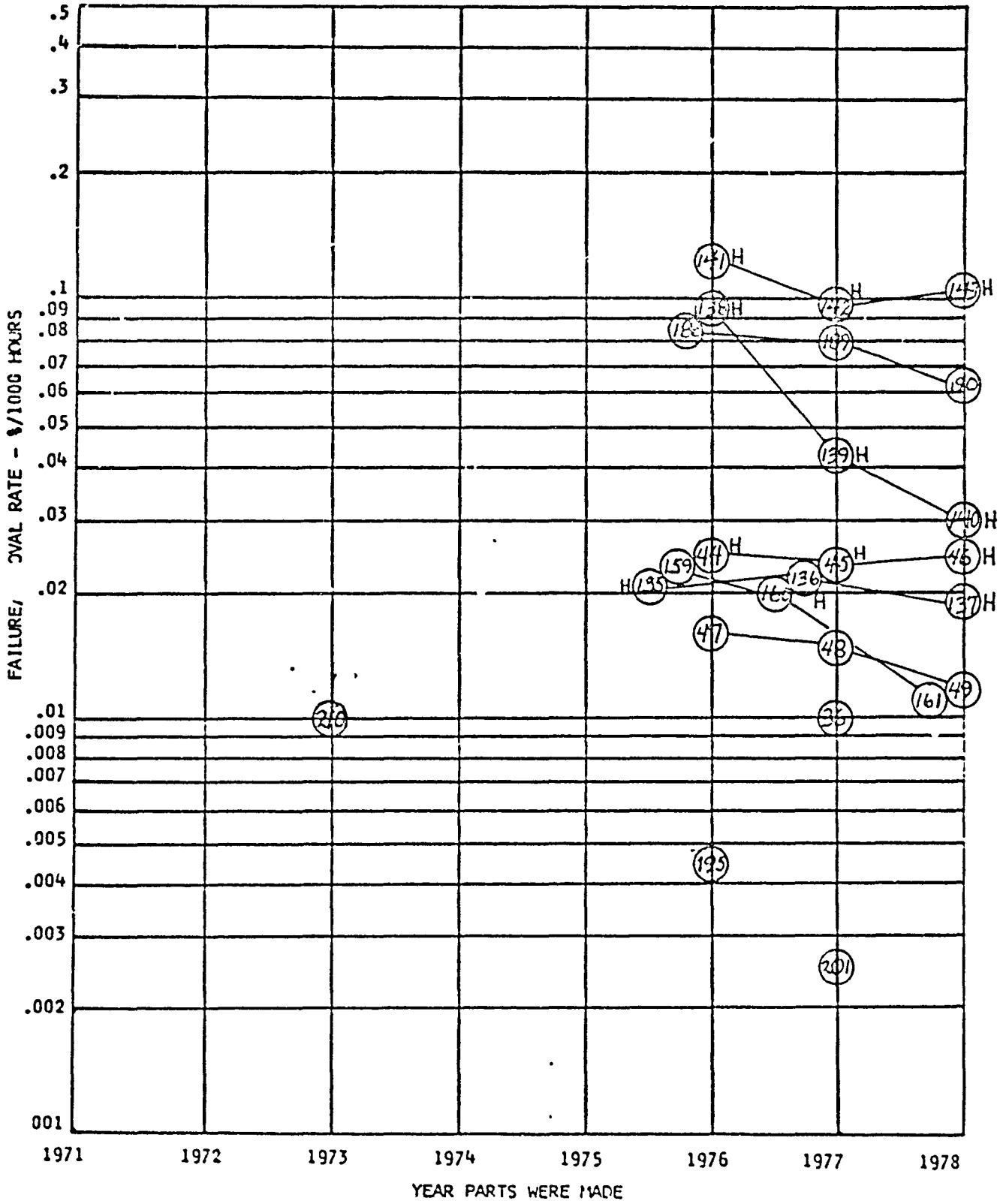


FIGURE 23. TRANSISTOR SS PNP

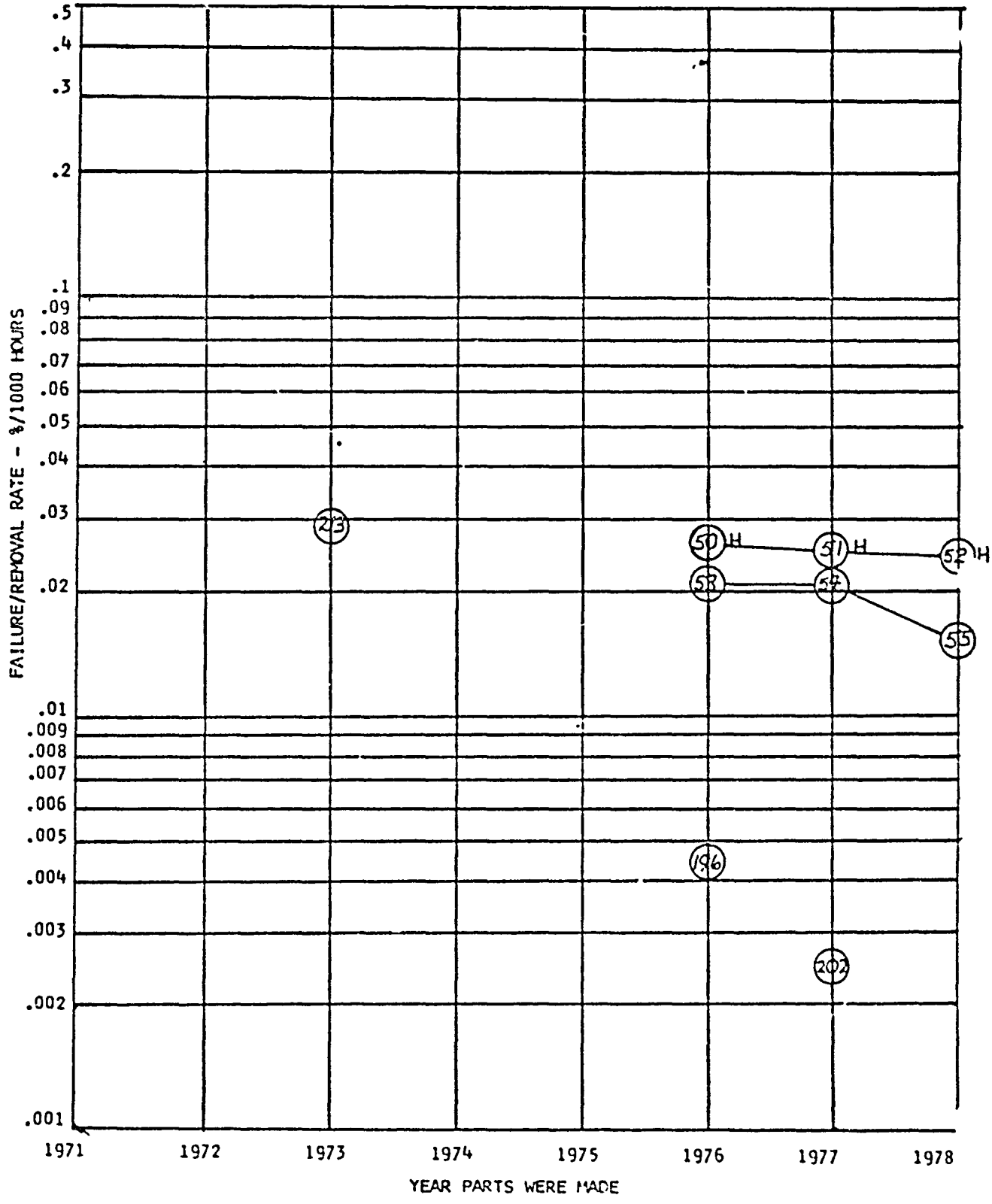


FIGURE 24. TRANSISTOR NPN POWER

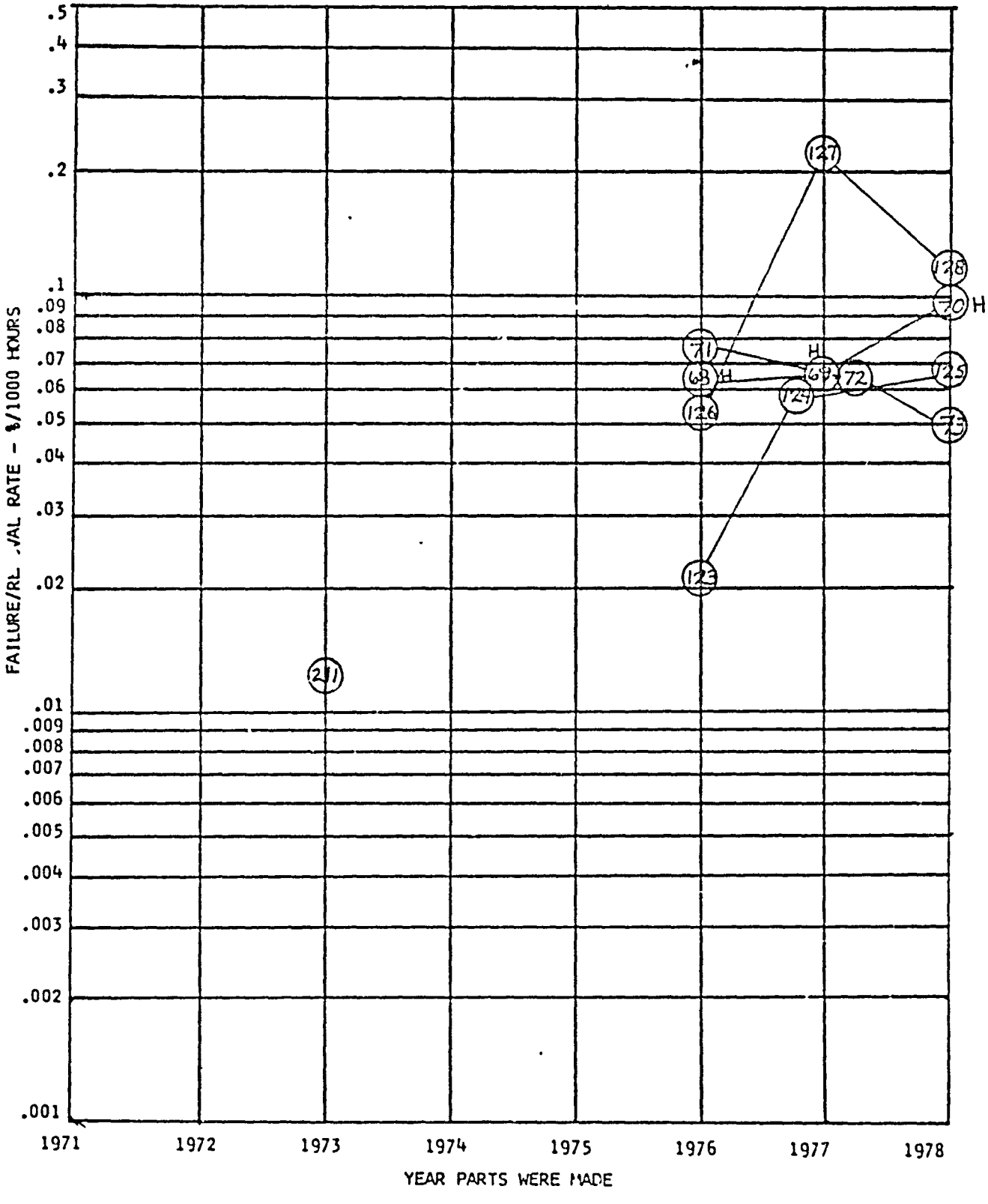
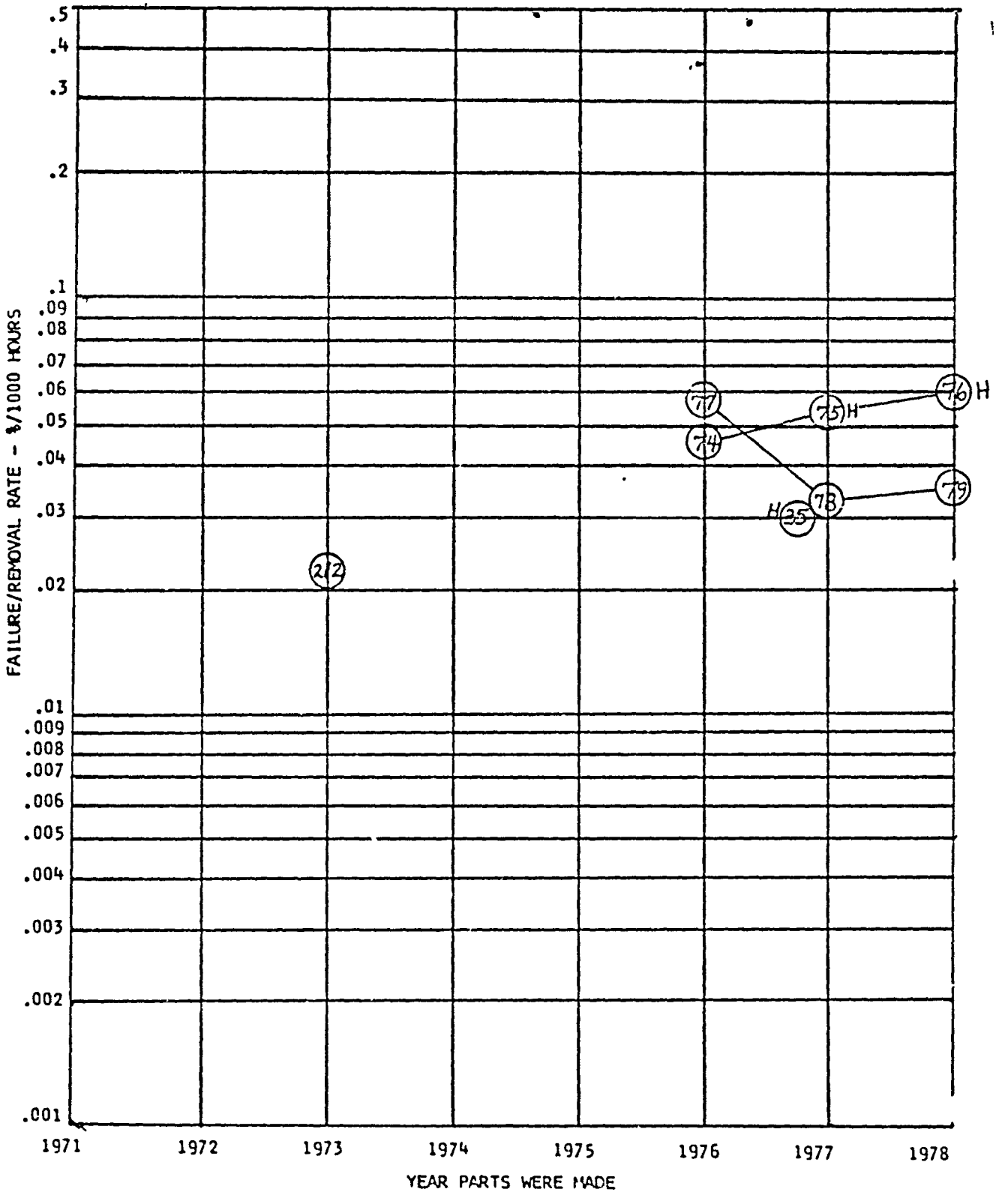


FIGURE 25. TRANSISTOR PNP POWER



D180-25325-1

FIGURE 26. SCR

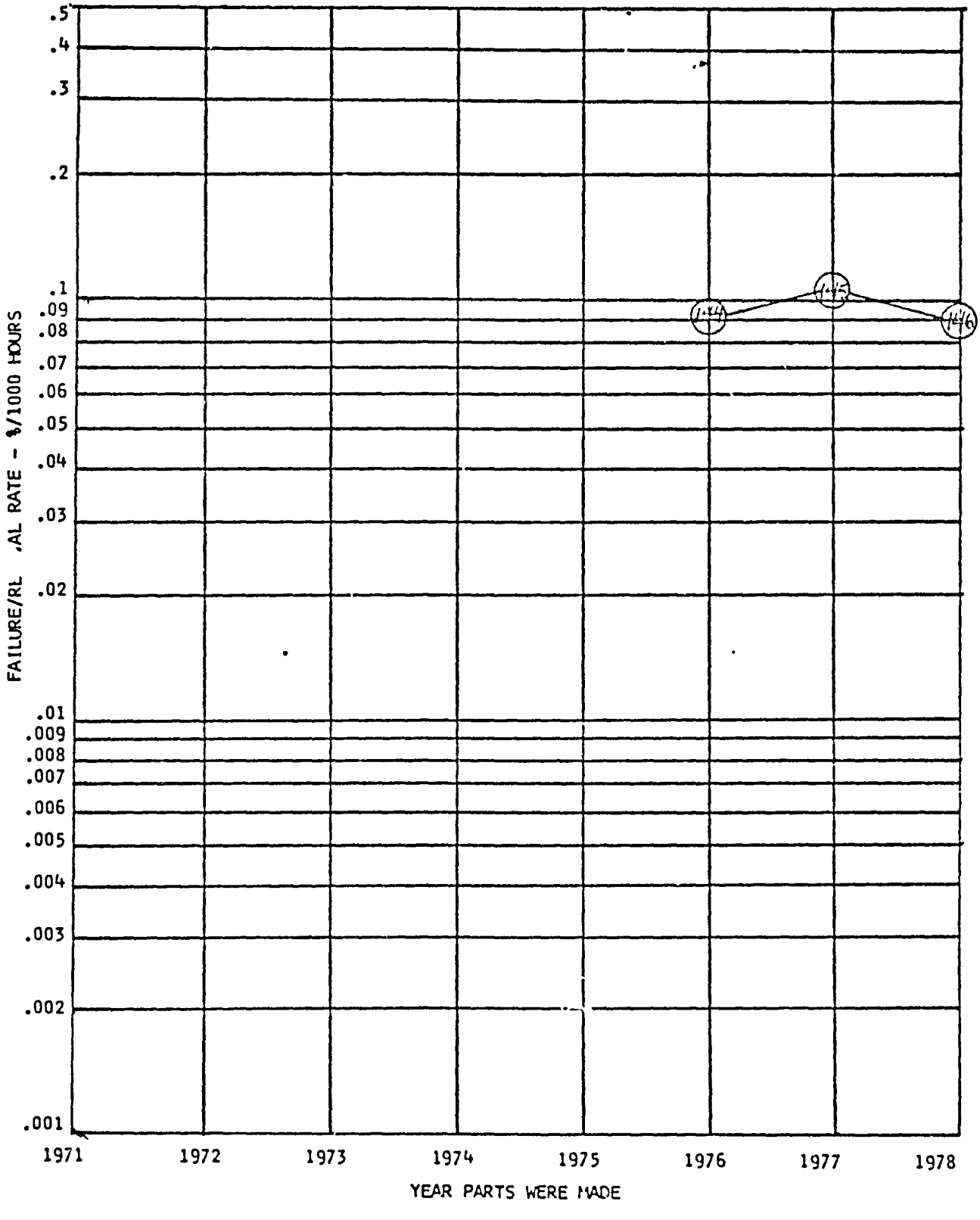


FIGURE 27. FET TRANSISTOR

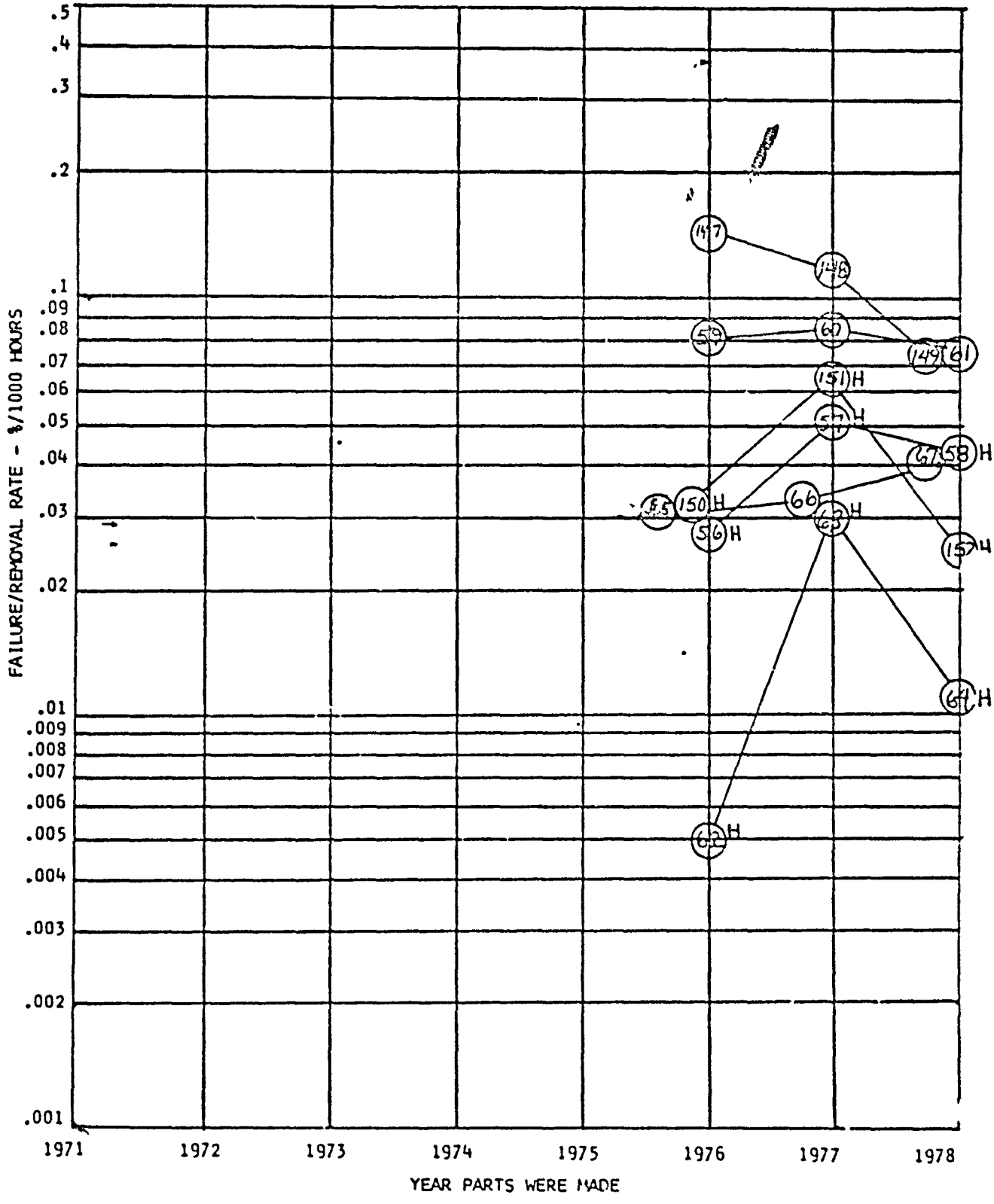
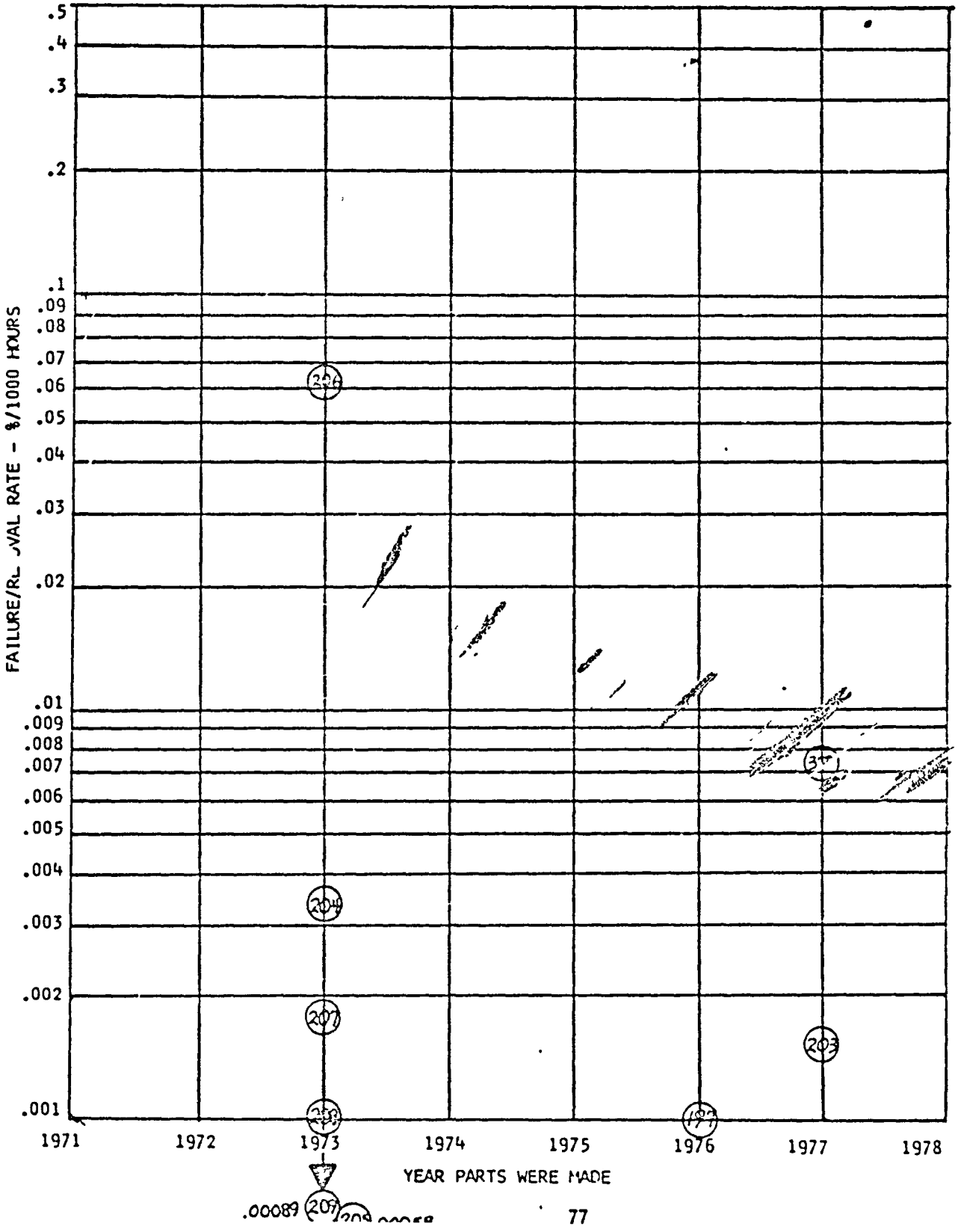


FIGURE 28. DIODES, SS, AND ZENER



5.3 Failure Rates Versus Technology and Screening

In order to make a comparison between the reliability of plastic encapsulated semiconductors and hermetically sealed semiconductors, several different summaries of the available data were performed. First, the data plots of Figures 1 through 28 were analyzed to determine the range of the failure rates for the most recent two years, 1977 and 1978. The results of this summary are shown in Tables 20 and 21. These tables also show the computed failure rate that could be expected if burn in were used giving a 5:1 improvement in failure rate.

Next, the data published by RAC were searched for comparable field data on hermetic parts that could be compared to the plastic encapsulated parts. Four categories of parts were found for which there were data on the JAN equivalent screening failure rates: bipolar SSI and MSI TTL, bipolar LSI STTL, and NMOS LSI.There were not enough data available to make the comparisons for any of the other categories. The RAC data covered parts that were qualified to JAN Class B, or which had been screened to the equivalent of JAN Class B (Categories 4, 5, and 6 in Table 5). The results of the RAC summary are shown in Table 22.

With these data in hand, it then became possible to construct a plot of the comparative reliability of plastic encapsulated microcircuits versus screened hermetic parts. Figure 29 shows these comparisons. For each category, the left hand box shows the results of the field usage data with no screening applied to the parts. The next box in each category shows the anticipated reliability that would result if the parts were burned in. The third box shows the prediction of the manufacturers for the reliability of the parts with no burn in. Note that the manufacturers seem to be very optimistic in their predictions, since their predictions seem to match closely the field usage data for burned-in parts, rather than for non-burned-in parts. Finally, the last box represents the RAC data for hermetic parts screened to JAN Class B. The failure rates for these parts are more comparable to the unscreened plastic encapsulated parts. The reason for this may be that the environment for the hermetic parts is much more severe. There is not enough information available for definitive identification of the reasons for the differences.

TABLE 20. Manufacturer Production of 55°C Failure Rate Range

Part Classification	Failure Rate With No Burn In: %/1000 hr Mfr. #	Min	Max	Failure Rate With Burn In: %/1000 hr Mfr. #	Min
Bipolar SSI					
TTL	2	.00068	.0041	2	.00035
TTL	1, 4	.C03		4	.00015
LSTTL	5	.0005		5	.00015
LSTTL	1		.003		
LSTTL	2		.0012		
Linear Amp	4	.0039	.0135	4	.0005
	1		.0125		
Bipolar MSI					
TTL	2	.0041		2	.0031
STTL	2	.0041		2	.0038
Bipolar LSI	4	.0088	.138		
CMOS SSI Logic	1	.0012	.005	1	.00088
NMOS LSI					
Logic (Microprocessor)	3	.0065			
	1		.037		
	7		.05		
Memory	3	.0051		3	.0023
	2	.013	.025		
	4		.0066		
	7		.05		

TABLE 21a. Summary of Microcircuit Field Usage Failure Rate Data (1977-1978)

Part Classification	Year	Actual Field Failure Rate Range in %/1000 hr. Min	Max	Expected Failure Rate Range If Burned In: %/1000 hr. Min	Max
Bipolar SSI					
TTL	1978	.0045	.03	.0008	.006
LSTTL	1978	.002	.005	.0004	.001
STTL	1977, 1978	.018	.033	.0036	.033
ECL	1978	.02	.04 (Hermetic)	.004	.008 (Hermetic)
Linear Amp	1978	.025	.09	.005	.0018
Linear Volt. Reg. (Fixed)	1978	.045	.075	.009	.015
Linear Volt. Reg. (Variable)	1978	.1	.15	.02	.03
Bipolar MSI					
TTL	1978	.013	.024	.026	.0048
LSTTL	1978	.004	.042	.001	.008
STTL	1977	.007	.045	.0014	.09
ECL (Hermetic)	1977, 1978	.036	.044	.0072	.0088
Bipolar LSI					
STTL (Hermetic)	1974	.03	.07	.006	.014
CMOS SSI					
Logic (Plastic)	1977, 1978	.01	.25	.006	.01
Logic (Hermetic)	1977, 1978	.03	.05	.002	.05
NMOS LSI					
Logic (Microprocessor)	1977, 1978	.05	.17	.01	.034
Memory	1977, 1978	.046	.07	.009	.014

TABLE 21b. Summary of Discrete Semiconductor Field Usage Failure Rate Data (1977, 1978)

Part Classification	Year	Actual Field Failure Rate Data in %/1000 hr. Min	Max	Expected Failure Rate Range if Burned in: %/1000 hr. Min	Max
Transistor Bipolar					
Small Signal NPN	1977, 1978	.0053	.08	.0011	.016
Small Signal PNP		.017	.025 (Hermetic)	.003	.005
Power NPN		.05	.13	.01	.026
Power PNP		.036	.06 (Hermetic)	.0072	.012
Transistor JFET					
Small Signal N Channel & P Channel		.045	.075	.009	.015

TABLE 22. Summary RAC Field Usage Data on Failure Rates of JAN Class B (or Equivalent) Hermetic Parts

Part Classification	Failure Rate %/1000 Hours Min	Max
Bipolar SSI TTL	.0022	.11
Bipolar MSI TTL	.0068	.15
Bipolar LSI TTL	.016	.71
NMOS LSI Memory	.087	.12

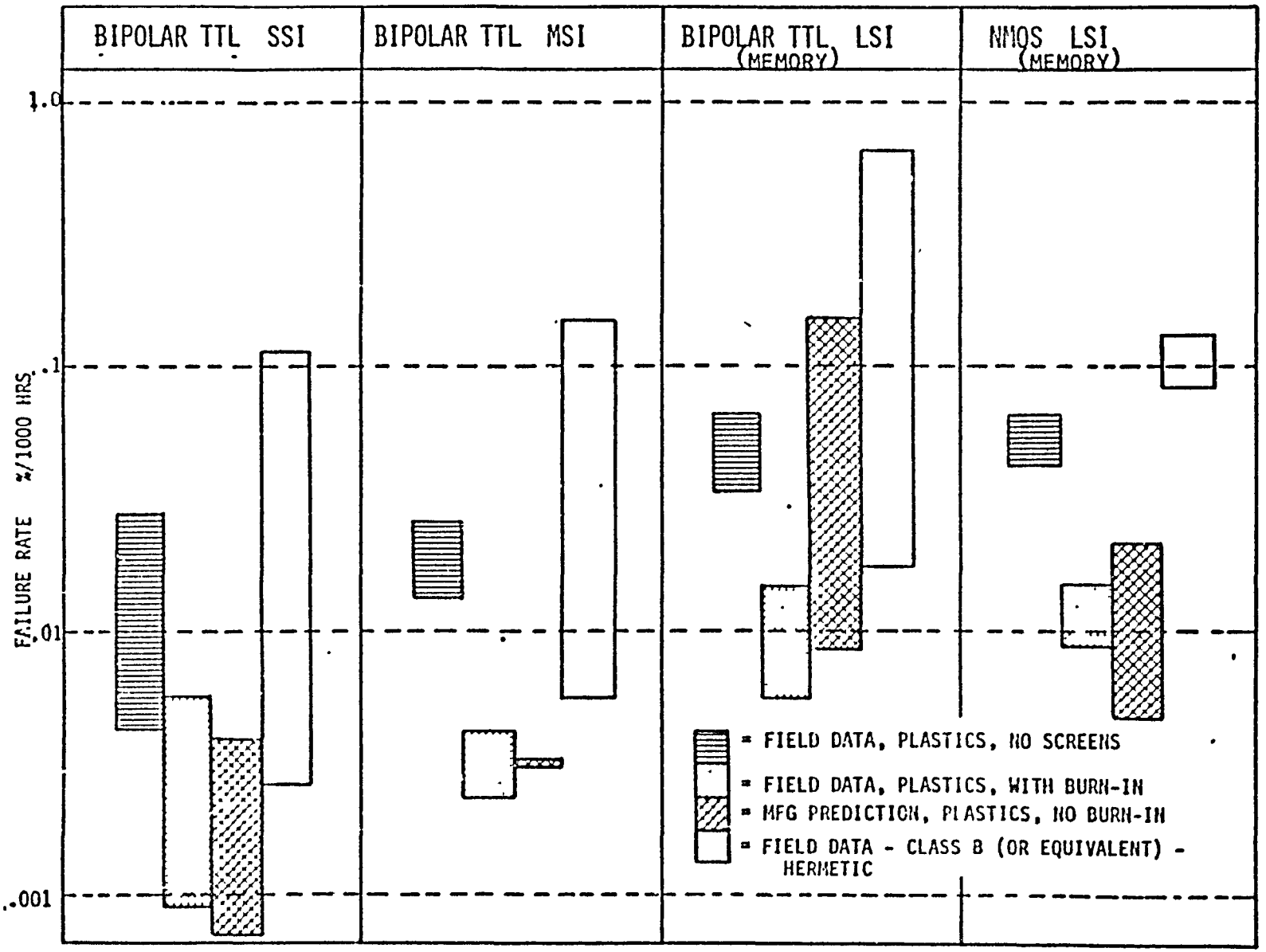


FIGURE 29 COMPARATIVE RELIABILITY OF PLASTIC ENCAPSULATED SEMICONDUCTORS

6.0 COST ANALYSIS AND COST FACTORS

6.1 Procurement Cost and Screening

One of the excuses for avoidance of plastic encapsulated semiconductors has been the position that by the time these parts are screened to the same level of rigor as the JAN parts they would be just as expensive and, therefore, there would be no point in their use. The experience of the users of plastic encapsulated semiconductors seems to contradict this in that these users have not found is necessary for employment of the rigorous screens of MIL-STD-883 to achieve the respectable reliability numbers they require in their systems.

In an attempt to get a handle on the cost picture, the manufacturers were interrogated during the plant visits concerning the additional costs that would be incurred to perform both the in-house screens and the proposed NASA Standard Flow screens listed in Table 28. In most cases, the manufacturers stated that firm cost figures could only be provided through the sales offices. For this reason, formal price estimates were requested from the manufacturers through Boeing Purchasing for budgetary pricing on 1000 quantity prices of a representative mix of semiconductor devices. Unfortunately, at the time of writing of this report, none of the manufacturers have responded.

A perspective on the cost picture can be reached, however, as a result of some of the informal pricing information that was obtained during the plant visits. Table 24 summarizes the pricing that was indicated by one manufacturer and can be used to draw conclusions as to the general posture of the manufacturers concerning pricing. In this table, it is seen that there are significant differences in the costs for the commercial temperature range plastic or hermetic parts compared to the JAN-qualified or JAN-equivalent-screened parts, both for the SSI parts and for the MSI parts.

In both cases, JAN screening costs 3 to 4 times as much as the standard in-house screening, and 2 to 2½ times as much as the proposed NASA Standard Flow. If it is assumed that low cost is the primary driver in the use of plastic encapsulated semiconductors, then the commercial temperature range hermetic parts are seen to be almost as cost effective. More important, though, is that the NASA Standard Flow is seen to be a reasonable priced alternative to JAN screening and could become a viable process for achieving low cost reliability assurance. However, it

SSI (54L/74L TYPE)	BASIC COST	ADDED FOR MFR IN-HOUSE REL SCREEN: TEMP CYCLE, BURN-IN 100% ELECTRICAL MEASUREMENT	TOTAL COST
PLASTIC (0-70°C)	.17	.25	.42
HERMETIC (0-70°C)	.19	.25	.44
HERMETIC (-55 - +125°C)	.30	$1.00 1/	$1.30
JAN CLASS B (-55 - +125°C)	$1.80	---	$1.80
PLASTIC (0-70°C)	.17	.39 2/	.56
MSI 54L/74L TYPE)			
PLASTIC (0-70°C)	$2.50	.35	$2.85
HERMETIC (0-70°C)	$3.00	.35	$3.35
HERMETIC (-55 - +125°C)	$4.00	$1.00 1/	$5.00
JAN CLASS B (-55°C - +125°C)	$6.00		$6.00
PLASTIC (0-70°C)	$2.50	.49 2/	$2.99

1/ 883B Screened

2/ Screened to a NASA Standard Flow. See Table 28A for proposed NASA Standard Flow.

TABLE 24 RELATIVE COST FACTORS FOR BIPOLAR MICROCIRCUITS

must be remembered that some manufacturers will refuse to bid on anything other than their in-house reliability screening and thus certain sources of supply would be lost by the imposition of the NASA Standard Flow. The solution to this would be the purch of unscreened parts with subsequent screening by screening laboratories using the NASA Standard Flow.

Probably the most important factor to be considered in the cost analysis of the use of plastic encapsulated semiconductors is that only those semiconductor devices that are in continuous production should be considered for use in low quantity NASA applications. The objective of low cost with reasonable reliability cannot be met for device types that are only produced sporadically or are essentially custom devices. All of the users visited stated that they only select device types and manufacturers that met the criteria of "continuous production".

- o Parts are in high volume production
- o Parts are available from more than one source
- o Parts are distributor stock items

This constraint should be particularly emphasized for NASA since the quantities of parts used on any one program are generally going to be very small compared to the production quantities of modern semiconductors. Where it is felt necessary to use part types that are only batch processed or are more custom oriented devices, NASA should decide that the cost consideration cannot enter in and ignore the cost advantages of plastic encapsulation, in the interest of assured reliability.

6.2 Cost of Parts Management and Control

An additional factor to be considered in the cost of plastic encapsulated semiconductors is the cost of the engineering staff required to perform the parts engineering and control functions associated with the procurement of reliability-assured parts. It turns out that a relatively small staff of parts engineers can perform the periodic qualification testing and manufacturer coordination necessary to maintain adequate control over the manufacturers of plastic encapsulated semiconductors. This might require a staff of 4 or 5 personnal, as seen to be used by many of the users.

However, if this staff must be duplicated for each contractor and subcontractor that attempts to use plastic encapsulated semiconductors, then the cost would become prohibitive. Either there must be set up a central NASA organization that would be responsible for the qualification and selection of manufacturers and part types, or

the tasks of qualification and manufacturer coordination must be distributed among the various contractors and subcontractors who are currently participating in NASA-contract programs.

7.0 QUALIFICATION REQUIREMENTS

7.1 Initial Qualification of Manufacturers Products

Qualification Considerations. In addition to the imposition of reliability screening requirements on plastic encapsulated semiconductors, it will be necessary to conduct qualification testing on all parts intended for use in deliverable electronics systems. Many of the users of plastic encapsulated devices have in-house programs of device qualification aimed at searching for possible lot oriented problems in the products being purchased.

The qualification approach recommended is one of comparative evaluation of the integrity of the products. This means that plastic encapsulated products would be purchased from several sources, subjected to qualification testing and then compared as to their relative performance capabilities in the qualification tests. Any manufacturer's product that is markedly poorer in the response to the tests would be eliminated from the set of parts to be used on the program.

Table 25 defines a set of qualification tests that have been suggested as useful by users and manufacturers of plastic encapsulated semiconductors. It is recommended that these tests be built into a NASA standard document for the control of the reliability of plastic encapsulated semiconductors.

The qualification process for a new part type will have to be tailored to each of the technologies considered for use in any NASA program. Different device types require different tests to be applied to uncover any unique process or performance anomalies. There are some basic qualification tests, however, that can be applied to all products in plastic packages. These are as shown in Table 25, consisting of autoclave (pressure pot) tests, temperature-humidity bias (85°C, 85% RH) and some form of high temperature operating life. In addition to these tests, certain device types would require exploratory testing using such stresses as temperature cycling, thermal shock, overvoltage stress testing, and extensive application of three temperature testing (-40°C, 25°C, and 125°C or 100°C) of electrical parameters and truth table functionality.

As an example of special tests that might be applied to perform qualification of different devices, it has been found by one user company that linear op amps can be accelerated to failure by application of a differential input of 24 volts to the

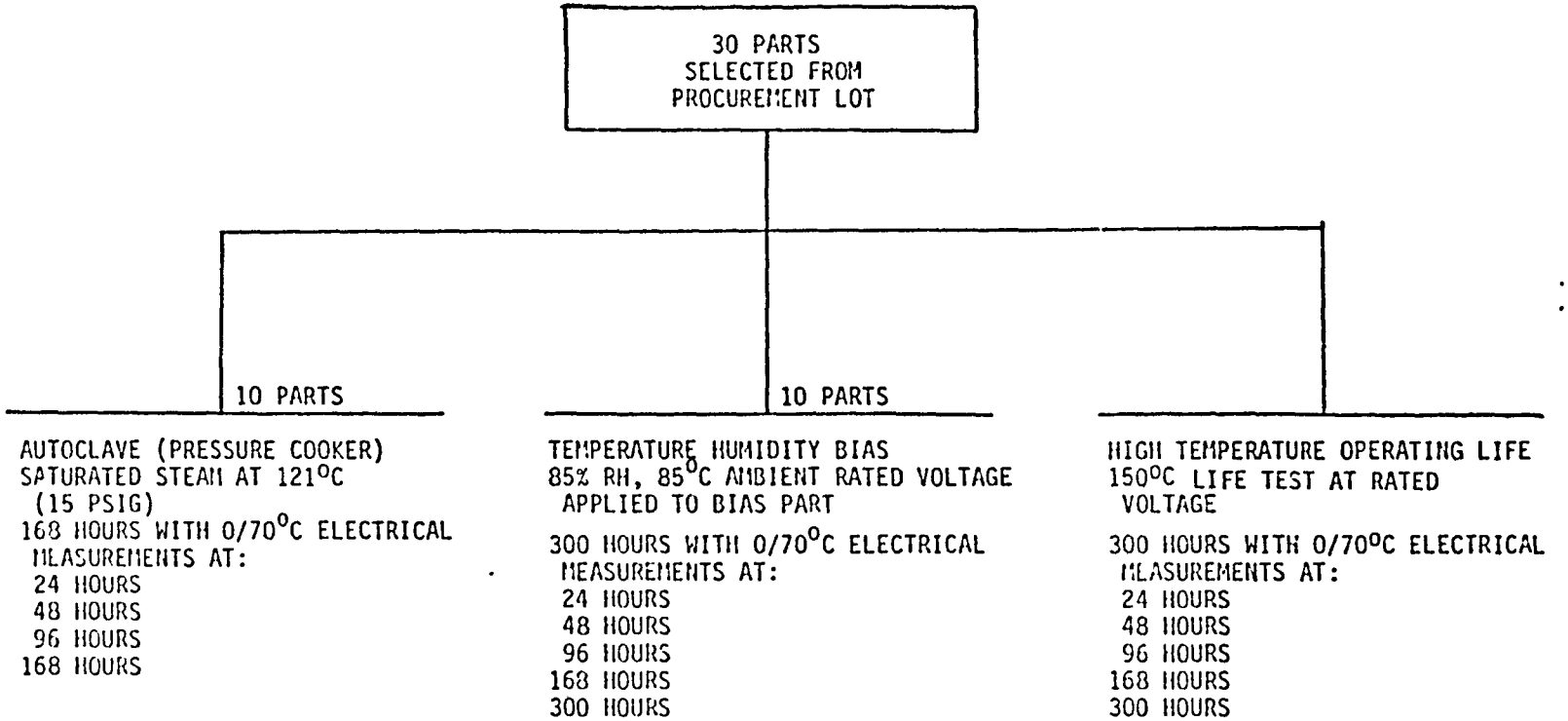


TABLE 25

LOT QUALIFICATION TESTS TO BE PERFORMED

input leads. This causes an acceleration factor of 1000 and can be used to compare the relative performance of different manufacturers products under identical test conditions. It is also recommended that delta measurements be made on linear microcircuit parameters. As another example, one manufacturer recommends that in addition to the Table 25 qualification tests, an effective qualification test for power transistors would be power cycling tests.

The reason for performing qualification tests is to obtain data to be used in evaluating the integrity of the various manufacturers' products. Most user companies that perform qualification tests compare the results from the different companies and reject the manufacturers whose products seem to deviate from the norm established by the other manufacturers. The decision as to the degree of deficiency must be made by parts engineering organizations on a case-by-case basis.

7.2 Continuing Qualification Testing

After the initial qualification of a manufacturer and his product, there must be established qualification procedures that will ensure that the reliability levels are maintained as a function of time. Most users achieve this by the periodic requalification of their purchased parts at intervals of approximately 9 months. At this interval, the initial qualification tests are repeated, with emphasis on searching for any differences in the device performance as compared to the previous testing.

Remembering that the users visited generally are using parts in quantities measured in the millions, the nine-month interval seems to be appropriate for them. However, for small lot procurement as is common for NASA, it would be necessary to invoke lot-by-lot qualification testing regimes. Typically, the parts for a project would all be purchased at the beginning of the program and, in the event that additional quantities had to be purchased, then the requirements of lot qualification could be reinvoked.

8.0 SCREENING CONSIDERATIONS

Once the parts from a particular manufacturer are qualified, then they must be 100% screened to assure the integrity of the parts. The two options that are available are the use of the manufacturers' in-house screening (such as "PEP 3" or "Better") or the use of a standardized screen that would be the same for all manufacturers.

8.1 Manufacturers' In-House Screens

Each part manufacturer has his own in-house screen he makes available as an extra cost option to purchasers of his parts. Table 26 summarizes the various screens performed by the manufacturers visited during the program. It can be seen that these screens differ widely from manufacturer to manufacturer, and no real standardization can be found. In addition, these screens are not available for all products from each of the manufacturers. Table 27 shows the products for which the in-house screening is available.

The only way that these screens can be obtained is to purchase the specific part number assigned by each manufacturer to his product that identifies the specific screen. This means that there is no single number to be called out on drawings that could result in similarly screened parts being purchased from different manufacturers. Thus, the use of manufacturers' in-house screens could only be used if a NASA project were willing to list all of the individual part number variations for a single part to cover the part from different manufacturers. This part number callout problem would exist even if there were no screening called for, because of the manufacturers unwillingness to develop any JEDEC numbering systems for microcircuits as they have for discrete semiconductors.

8.2 NASA Standard Flow

As a result of the discussions with the manufacturers during the plant visits, it was possible to define certain relatively universal screens that a majority of the manufacturers might be willing to perform instead of their normal in-house screens. This definition was determined by discussion of the cost factors of performing "nonstandard" (to the manufacturer) screens and the capability to communicate the screen test parameters to their offshore test facilities where the screening is performed. Tables 28A and B spells out the proposed NASA Standard Flow screening procedure that might have a tolerable degree of acceptability to the

PROGRAM / SCREEN	MANUFACTURER (1)	MANUFACTURER (2), LEVEL 3		MANUFACTURER (3) LEVEL A	MANUFACTURER (4) LEVEL B	MANUFACTURER (5) LEVEL 2	MANUFACTURER (6) LEVEL 5
		DIGITAL	LINEAR BI-MEM				
HIGH VOLTAGE STRESS AT WAFER PROBE			YES				
PRECAP VISUAL		YES			YES	YES	YES
TEMP CYCLE	10cy,-25/150°C	10cy,0/100°C		5cy, 0/100°C air to air	15cy,0/100°C Water shock	15cy 0/100°C Liquid shock	15cy 0/100°C Water shock
Continuity (I_{cc})		100°C					
Functional	100°C	100°C	25°C	25°C		25°C	25°C
DC PARAMETERS		100°C	25°C	25°C		25°C	25°C
BURN-IN	40hrs @ 145°C or 168hrs @ 125°C	21hrs @ 155°C		40hrs @ 150°C	24hrs @ 155°C	168hrs @ 125°C or 80hrs @ 150°C	168hrs @ 125°C
FUNCTIONAL	25°C	70°C	25°C	100°C, 25°C	100°C, 25°C	100°C	100°C
DC PARAMETERS	25°C	70°C	25°C	25°C	25°C	25°C	25°C

TABLE 26 COMMERCIAL HI-REL BASELINE SCREENS

PROGRAM	BIPOLAR SSI	LINEAR	BIPOLAR MSI	BIPOLAR LSI		CMOS	NMOS LSI		TRAN-SISTOR	DIODE
	TTL,LSTTL,ECL		TTL,LSTTL,ECL	RAM	LOGIC		μP	RAM		
MANUFACTURER (1)	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO
MANUFACTURER (2)	YES	YES	YES	NO	YES	--	NO	NO	NO	NO
MANUFACTURER (3)	YES	YES	YES	NO	YES	NO	NO	NO	LEVEL B ONLY	--
MANUFACTURER (4)	YES	YES	YES	NO	YES	--	NO	NO	--	--
MANUFACTURER (5)	YES	YES	YES	NO	NO	--	--	--	--	--
MANUFACTURER (6)	YES	YES	YES	YES	NO	YES	NO	YES	NO	NO
MANUFACTURER (7)	--	--	--	--	NO	--	NO	NO	--	--

YES MEANS YES, APPLIES TO THIS PRODUCT
NO MEANS DOES NOT APPLY TO THIS PRODUCT
-- MEANS NO PRODUCT IN THIS CATEGORY

TABLE 27

COMMERCIAL HI-RELIABILITY SCREENING PROGRAMS

TEMPERATURE CYCLING	30 CYCLES: $0^{o}C$ to $100^{o}C$, GAS TO GAS
100% FUNCTIONAL TEST	$70^{o}C$, $25^{o}C$
100% DC PARAMETERS	$70^{o}C$, $25^{o}C$
BURN-IN	168 HOURS AT $125^{o}C$ (OR EQUIVALENT USING 1.0ev ACTIVATION ENERGY) $\theta < 150^{o}C$
100% FUNCTIONAL TEST PERFORMED TWICE (TWO PASSES)	$70^{o}C$ $25^{o}C$
100% DC PARAMETERS TEST PERFORMED TWICE (TWO PASSES)	$70^{o}C$ $25^{o}C$

TABLE 28A

PROPOSED NASA STANDARD FLOW FOR
RELIABILITY SCREENING OF PLASTIC ENCAPSULATED MICROCIRCUITS

SCREEN	POWER TRANSISTORS	SMALL SIGNAL TRANSISTORS	ZENER DIODES	RECTIFIERS
TEMPERATURE CYCLING	30 CYCLES 0 TO 100°C (GAS TO GAS)			
100% FUNCTIONAL AND PARAMETRIC TESTS	70°C AND 25°C			
100% SPECIAL OVERSTRESS SCREEN	SAFE OPERATING AREA (SOA): VBEF AT RATED I_C 300μsec	VBEF AT RATED I_C: 300μsec	SURGE TEST: 100ms PULSE, 10% RATED POWER OF DIODE	HTRB 48 HR @ 125°C
100% PARAMETRIC TESTS (TWO PASSES AT EACH TEMPERATURE)	70°C AND 25°C			

TABLE 28B

PROPOSED NASA STANDARD FLOW FOR RELIABILITY SCREENING OF PLASTIC ENCAPSULATED DISCRETE SEMICONDUCTORS

manufacturers. Several of the manufacturers indicated that they would not be interested in performing any screens that they do not have covered by their in-house screening program. It must be noted that there was no full commitment by any manufacturer to perform the NASA Standard Flow screens. Such a commitment could only be obtained by direct contractual negotiation with each of the manufacturers involved.

8.2.1 Temperature Cycling

There was evidence put forth by Manufacturer (1) indicating that 30 cycles of temperature cycling does a significantly better job of intercepting weak bonds than does just 10 cycles. This manufacturer also indicated that water-to-water thermal shock should be avoided because of the possibility of introduction of water into the package by such a process. This manufacturer also believes in the temperature cycling temperature range of -75°C to +150°C, but this would impose severe problems to the other manufacturers who universally use 0°C to 100°C. Thus, the use of 30 cycles, from 0°C to 100°C, gas to gas is the preferred temperature cycling screen.

8.2.2 100% Pre-Burn-In Electrical Measurement

The manufacturers perform functional test and parametric measurement to differing temperatures. It was decided that pre-burn-in measurement is an important test and should be performed both at 70°C and 25°C, with functional test (truth table test) and DC parameters both being measured at both temperatures. The basic intent of all of the electrical measurements is to screen out the parts that have defects built into them at the outset.

8.2.3 Burn In

For microcircuits, standard static burn-in techniques should be used to subject all parts to 100% burn in. Static burn in is recommended for two reasons. First, it provides the capability to detect migration and inversions; and second, it is much easier and much cheaper than dynamic burn in. Instead of 168 hours at 125°C, many manufacturers employ accelerated testing that assumes a 1.0ev activation energy, and this results in such variations such as 40 hours at 145°C or 21 hours at 155°C. Any of these equivalent arrangements would be permissible as long as the junction temperature is restricted to less than 155°C for linear and MOS and 175°C for bipolar digital.

C-2

For discrete semiconductors, none of the manufacturers provide for burn in with their in-house screen programs. Instead, a variety of special screens were recommended, because they were felt to be more effective in intercepting problem parts than was burn in.

For power transistors, the manufacturers recommend that all devices be tested for Safe Operating Area (SOA) at one point on the characteristic curve to ensure that there are not problems with the die attach, and that they receive a 300 microsecond pulse of rated collector current applied to the base-emitter junction to look for bad wire bonds.

For small signal transistors, the VBEF test is again recommended, again performed at the rated collector current. Zener and reference diodes should be subjected to a 100 millisecond 20 watt surge test to look for oxide faults. Full power burn in of 1 watt for 48 hours is felt to be most effective but is too costly in the large quantities and is generally avoided.

For rectifiers, there is no one special test felt to be most effective. For blocking voltage applications, HTRB is felt to be the most effective screen, but for AC rectifier applications HTRB is not felt to be important. The recommended duration of HTRB is 48 hours at 125°C.

8.2.4 Post-Burn-In Electrical Measurements

Following burn in, electrical measurement of the truth table and DC parameters should be made not once but twice at both 70°C and 25°C. This means a total of four passes through the tester, and more if functional testing must be done separately from DC parameter testing.

The reason for the double testing is that it has been found that each pass through the tester can yield a significant number of escapes of parts that test good but are in fact defective. In general, approximately 10% of the reject parts escape detection at any pass through the tester. User B indicated that after the first pass through the tester there would still be 0.1% bad parts in any given lot of parts. By subjecting the lot to a second pass through the tester the number could be reduced to 0.01% (this is 100 parts per million) and it would take a third pass to reduce the percent defective to .001% or 10 parts per million, the number that

is being achieved by the Japanese. On this basis, it was determined that two passes would be the minimum number allowable for NASA parts, with the additional proviso that the testing also be performed twice at 70°C.

As can be seen from Table 24, the additional cost for screening commercial plastic encapsulated parts to the NASA Standard Flow would be only $.39 to $.49, depending on the relative complexity of the parts. This dollar figure must be firmed up for each of the various part types, however, and should not be used as a general indicator for all part types.

APPENDIX A

USER DATA REPORTS

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User A Data Report

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NOVOLAC PLASTIC BIPOLAR IC STUDY

FIELD PHASE

FINAL REPORT

FEBRUARY 17, 1978

Prepared By: _____
Novolac Plastic Bipolar
IC Study
Program Manager

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PURPOSE

The purpose of this study was to:

Determine the failure rate of bipolar ICs encapsulated in Novolac plastic packages.

INTRODUCTION

This report summarizes the field phase results of the Novolac Plastic Bipolar IC Study. The field phase involved monitoring Novolac encapsulated ICs from four vendors identified as A, B, C, and D in equipment, the MP which was designed by Company 1 and manufactured by both Company 1 and Company 2, that has been installed in the field. The circuits selected for this evaluation were standard TTL SSI and MSI circuits, high speed TTL SSI and MSI circuits and Schottky TTL SSI and MSI circuits.

Nine different types of MP related Printed Wiring Assemblies (PWAs) were selected as the vehicle to perform the evaluation. All PWAs of the nine types manufactured between 6/1/74 and 6/1/77 by either Company 1 and Company 2 became a part of this evaluation. A sample of four hundred and ninety (490) PWAs were metered with elapse time meters have a range of ten thousand (10,000) hours. All meters were installed between 1/1/75 and 3/1/76.

Although failure information was obtained on all PWAs, metered and not metered, the failure rate for Novolac encapsulated bipolar ICs established by this report is based solely on the metered PWAs. The failure information on the PWAs not metered is included to support these findings.

For the purpose of this report, the collection of failure data was discontinued on 8/1/77 with the final meter readings being taken in January of 1978. The operating environment, although originally expected to be various, resulted in almost totally computer room environment domination. Therefore, for the purposes of this report, all conclusions are more applicable to a computer room environment than other categories of environments.

CONCLUSIONS

1. The failure rate of Novolac encapsulated Integrated Circuits (ICs) with protective die glass passivation is calculated to be 0.04 failures per million device hours at a 60% confidence level.

2. The failure rate of Novolac encapsulated ICs without protective die glass passivation is calculated to be 0.2 failures per million device hours at a 60% confidence level.

3. No broken wires due to the expansion/contraction properties of the materials making up a Novolac plastic encapsulated IC were found. Therefore, the intermittent open failure mode previously associated with Plastic packages is no longer a major failure mode.

4. No metal corrosion was in evidence in Novolac plastic encapsulated ICs that had a protective glass passivation over the die; however, for die that does not have a glass passivation metal corrosion is the major failure mechanism.

5. The failure information from the PWAs that were not metered supports the findings of this study.

TEST RESULTS

GENERAL

During the period of 6/1/74 through 6/1/77, 3399 of the nine types of MP PWAs were manufactured. 490 of these were metered for the purpose of accumulating device hours so as to accurately predict the failure rate of Novolac encapsulated bipolar ICs. The 3399 PWAs represent 394,203 bipolar ICs. The 490 metered PWAs represent 13% of this count. See Appendix I, Tables I and II for details of the IC distribution by PWA type, package type and manufacture.

All PWAs returned to Company 1 for any type of disposition were tracked from receipt until final disposition. Table I is a summary of all PWAs, by PWA type, returned to Company 1 during the period 6/1/74 through 8/1/77.

TABLE I RETURNED PWA SUMMARY BY ASSEMBLY TYPE

Assembly	FAILURES				
	No.of PWAs Built	No. of * PWAs Returned	No. of Failures	No. of ICs Replaced	Remarks
ALU	415	86	49	45	Includes 17 82S16 RAM failures.
Control 1	365	57	29	19	24 PWAs returned for ECO update.
Control 2	583	54	30	27	9 PWAs returned for ECO update
SMI	545	31	14	14.	
Transform	323	160	51	34	Includes 18 82S115 PROMS
Memory I/F	117	13	0	0	
Panel I/F	492	69	31	27	Includes 9 82S123 PROMS
I/O TTY	248	84	32	26	
CP/LP	311	15	8	7	
TOTALS	3399	569	244	199	

* Includes multiple returns of the same PWA

The three bipolar devices referenced in the remarks section of Table I were specifically excluded from the study at the onset because of potential problems associated with each device type. The 82S16, a 256 X 1 RAM, was undergoing a design change due to a problem which resulted in device pattern sensitivity, the 82S123, a 32 X 8 PROM, was subject to pattern changes throughout the study and both devices dissipated in excess of 600 MW of power. The 82S115 is a 24 pin 512 X 8 PROM and was supplied in ceramic and CERDIP only.

Table II is the same data summary information organized by returning organization.

The purpose of Tables I and II is solely to show the amount of activity that occurred over the length of the program. This data is strictly raw return data. That is, it includes PWAs returned for Engineering change only, returned with no problems found, returned that had ICs with propagation delay problems and returned with non-IC problems. The pertinent bipolar IC failure data is contained in the next two portions of this section.

TABLE II RETURNED PWA SUMMARY BY ORGANIZATION

Facility	Totals	NPF	IC	Non-IC	Missing 1/
* CEM	211	104	68	23	16
* STAOPS	259	129	107	19	4
* VF	50	40	9	1	0
* LJLOPS	14	8	4	2	0
* Others	35	23	11	0	1
Total	569	304	199	45	21

NPF = No Problem Found

1/ 3 of the 21 missing Failure Reports are from metered PWAs. (Two Transforms and one ALU)

METERED PWAs

The 490 PWAs metered for this study resulted in 51,122 ICs being monitored with the four principle vendors (A, B, C, and D) accounting for 95% of the total sample. Table III is a summary of the vendor/package distribution and Table IV gives each vendor's percentage of contribution by package type.

TABLE III.
VENDOR/PACKAGE DISTRIBUTION OF THE ICs USED IN THE 490 METERED BOARDS

PACKAGE	VENDOR											
	A		B		C		D		OTHERS		TOTALS	
	#	%	#	%	#	%	#	%	#	%	#	%
Novolac	13,912	27.2	16,388	32.1	5,487	10.7	6,562	12.8	1,786	3.5	44,135	86.3
Cerdip	5,909	11.6	170	.4	24	0	8	0	546	1.1	6,657	13.1
Others	37	0	10	0	1	0	73	0.1	209	0.4	330	.6
Totals	19,858	38.8	16,568	32.4	5,512	10.8	6,643	13.0	2,541	5.0	51,122	100.0

TABLE IV VENDOR % OF THE TOTAL SAMPLE BY PACKAGE TYPE

Package	% Of Total Sample				TOTAL (%)
	A	B	C	D	
Novolac	31.5	37.1	12.4	14.9	95.9
Cerdip	88.6	2.7	0.4	0.1	91.8

As can be seen by Table III Novolac accounts for only 86.3% of the total sample. The CERDIP sample, accounting for 13.1%, thus allows for a comparison of the two types of packages in the same operating environment.

The first PWAs were metered and mapped in January of 1975 with the last PWA metered and mapped in March of 1976 (a IC placement chart was filled out for each of the 490 monitored PWAs; information included vendor, date code and package type). Since there were two manufacturing facilities involved with the MP program PWAs from both facilities were included as part of the monitored sample. Table V is a summary of the monitored PWAs manufactured by the two facilities as well as a summary of the failure information accumulated on these PWAs.

TABLE V

SUMMARY OF COMPANY L AND COMPANY 2
METERED PWAs

Assembly Generic Name	Metered PWA Quantities								
	Manufactured			Returned			Problems Found		
	CO.1	CO.2	Total	CO.1	CO.2	Total	CO.1	CO.2	Total
ALU	32	24.	56	10	8	18	4	3	7
Control 1	46	24	70	10	5	15	6	4	12
Control 2	30	41	71	8	13	21	1	9	14
SMI	34	39	73	4	4	8	1	4	5
Transform	29	29	58	18	16	34	5	6	11
Memory I/F	1	13	14	0	1	1	0	0	0
Panel I/F	42	31	73	16	2	18	10	2	12
I/O TTY	26	34	60	6	16	22	3	7	10
CR/LP	7	8	15	3	3	6	2	2	4
TOTAL	247	243	490	75	68	143	36	39	75

As can be seen from Table V that the metered PWAs were evenly distributed between the two companies and the number of PWAs returned and the number of problems found were approximately the same. The following is a description of all of the failure information by PWA type and Table VI summarizes this information.

Control 1

The 70 Control 1 PWAs accounted for 8 IC failures and 4 non-IC failures. Two of the ICs (74H10 and 74175) were infant mortality failures with 100 and 300 hours respectively. Of the useful life failures five were SSI circuits (74H08(2), 74H10, 7414, 74H20) and one was an MSI circuit (74H74). The failures occurred at 4200, 7500, 3500, 5400, 3400 and 1000 hours respectively. The 74H74 failure was in a CERDIP package.

Control 2

The 71 Control 2 PWAs accounted for 13 IC failures and 1 non-IC failure. Two of the ICs (74136 and 74S175) were infant mortality failures with 300 hours on each, one was an Epoxy "A" package (74S175) which failed at 300 hours, six were 74191s with AC problems and two 74155s had supply margin sensitivity problems (both were marginally good). Of the useful life failures all were MSI circuits (74155(2), 74156, 74191, 74S175). The failures occurred at 900, 10,000, 2000, 1500 and 3000 hours respectively. The 74191 was in a CERDIP package.

SMI

The 73 SMI PWAs accounted for 5 IC failures. One of these, a 74175 was an infant mortality failure which had 300 hours on it. Also a 74175 was removed which had 3300 hours on it but could not be verified as a failure by DSLD or CQL. Of the useful life failures two were SSI circuits (74H51 and 7437) and one was an MSI circuit (74175). The failures occurred at 2000, 2000 and 3300 hours respectively. The 74H51 was in a CERDIP package.

Memory I/F

No failures were recorded against the 14 PWAs.

Panel I/F

The 73 Panel I/F PWAs accounted for 8 IC failures and 4 non-IC failures. Two of the failures (9309 and 82S123) were infant mortality failures with 10 and 50 hours on them respectively. One failure, a 74161, with 600 hours on it could not be verified by DSLD or CQL, one was a 82S123 with 2500 hours on it (82S123s were excluded from the study) and one failure, a 9602, with less than 10 hours on it was an AC failure. Of the three useful life failures, one was an SSI circuit (74H51) and two were MSI circuits (9309 and 74194). The failures occurred at 1400, 3500 and 6500 hours respectively.

Transform

The 58 Transform PWAs accounted for 7 IC failures and 4 non-IC failures. Three of the failures were 82S115 failures. Of the four useful life failures one was an SSI circuit (74H04) and three were MSI circuits (74151(2) and 74150). The failures occurred at 500, 1500, 3000 and 1000 hours respectively.

ALU

The 56 ALU PWAs accounted for 7 IC failures. One of these, a 7489 with 500 hours on it was in an Epoxy "A" package, one was a 82S16, one, a 74151, had an AC problem, one, a 74S181 with 300 hours on it, could not be verified by DSLD or CQL and one, a 74S194, was an infant mortality failure with 200 hours on it. Of the two useful life failures one was an SSI circuit (7402) with 500 hours on it and the other an MSI circuit, 74175, in a CERDIP package with 600 hours on it.

I/O TTY

The 60 I/O TTY PWAs accounted for 10 IC failures. Two, a 74H00 and a 74H04, with 100 hours on each of them were infant mortality failures. Of the eight useful

life failures four were SSI circuits (74H20(3) and 74H10) and four were MSI circuits (74175(4)). The failures occurred at 900, 900, 900, 5000, 6000, 6000, 1000 and 3500 hours respectively.

Card Reader/Line Printer

The 15 CR/LP PWAs accounted for four failures, all useful life failures. Two were SSI circuits (74H00 and 74H04) and two were MSI circuits (74157 and 74175). The failures occurred at 3700, 8000, 4000 and 4000 hours respectively. The 74157 was in a CERDIP package.

TABLE VI METERED PWA FAILURE SUMMARY

Assembly	No. of ICs Replaced	No. of Non-ICs Replaced	Non-Catastrophic IC Replacement	Infant Mortality		Useful Life Failures SSI	MSI	LSI
C1	8	4	0	2	7700	5	1 ceridip	0
C2	13	1	8	2	7810	0	3 (1 ceridip)	0
SMI	5	0	1	1	8030 7883	2 (1 cerdip)	1	0
MI/F	0	0	0	0	1540	0	0	0
PI/F	8	4	3	2	8030	1	2	0
Tx	7	4	3	0	6380	1	3	0
ALU	7	0	4	1	6760	1	1 ceridip	0
I/O TTY	10	0	0	2	6600	4; 1 ea 5000	4 1,600 1,1000 1,3500	0
CR/LP	4	0	0	0	1650	2 3700 5000	2 1 cerdip 4000 hrs	0
TOTALS	62	13	19	10	53900	16	17	0

58/22

15 Plastic SSI
1 cerdip SSI
13 plastic MSI
4 cerdip MSI

PWAs NOT METERED

There were a total of 2909 PWAs of the nine MP types manufactured between the period of 6/1/74 and 6/1/77. 426 were returned for various reasons, including ECO updates, with 176 problems found of which 137 were IC replacements (see Table VII for details). Removing the failures from the three ICs described in Table I and the 74S194 and 74194 AC problems associated with the ALU PWA there was 89 suspected functional and/or parametric failures with six of these being CERDIP failures. The following is a description of all of the failures information by PWA type and Table VIII summarizes this information.

Control 1

The 295 Control 1 PWAs accounted for 11 IC failures (10 Novolac and 1 CERDIP) and 6 non-IC failures. The IC failures were seven SSI circuits (74H08(4), 74H04, 74S04, 74S11) and four MSI circuits (74H74(2), 8214(2)). All IC failures were verified to be functionally and/or parametrically defective however none of the circuits were failure analyzed.

Control 2

The 512 Control 2 PWAs accounted for 14 IC failures and 2 non-IC failures. The IC failures were two SSI circuits (74S04, 74H10) and twelve MSI circuits (74191(3), 74156(3), 74S175(3), 9309, 74157, 74H74). All IC failures were verified to be functionally and/or parametrically defective, however, none of the circuits were failure analyzed. The 74191 failures were AC parameter failures.

SMI

The 472 SMI PWAs accounted for 9 IC failures. These failures were two SSI circuits (7437, 74H04) and seven MSI circuits (74175(3), 74H74(2), 74S175, 9318).

All failures were verified as functional and/or parametric failures however, none were failure analyzed.

Memory I/F

No failures were recorded from the 103 Memory I/F boards.

Panel I/F

The 419 Panel I/F PWAs accounted for 19 IC failures. These failures were four SSI circuits (74H01(2), 74H00, 74H51) and fifteen MSI circuits (82S123(7), 74161(3), 7486, 74174, 74175, 9602). All failures were verified as functional and/or parametric failures. Two circuits were failure analyzed and both were found to contain oxide defects.

Transform

The 265 Transform PWAs accounted for 27 IC failures and 13 non-IC failures. The IC failures were three SSI circuits (74H04, 74S00, 74H00), nine MSI failures (8123(5), 74174, 74S175, 74157, 74150) and fifteen LSI circuits (82S115(15)). All SSI and MSI failures were verified as functional and/or parametric failures. One circuit was failure analyzed and found to contain a mask defect.

ALU

The 359 ALU PWAs accounted for 38 IC failures and 4 non-IC failures. The IC failures were two SSI circuits (74H04(2)), sixteen MSI circuits (74194(6), 74S194(3), 9309(3), 74175(2), 74S182, 8214) and twenty LSI circuits (82S16(17), 74S181(3)). The 82S16 RAMS, as previously stated, were found to be pattern sensitive problems and the 74194/74S194 problems were found to be AC problems associated with a left or right shift operation.

I/O TTY

The 188 I/O TTY PWAs accounted for 16 IC failures and 6 non-IC failures. The IC failures were four SSI circuits (74H21, 74H00, 7407(2)) and twleve MSI circuits (74175(3), 8214(3), 74161(2), 74191, 7497, 74H74).

Card Reader/Line Printer

The 296 CR/LP PWAs accounted for 3 IC failures and 1 non-IC failure. The IC failures were two SSI circuits (74H04(2)) and one MSI circuit (9615).

TABLE VII

RETURNED PWA STATUS

Item No.	PWA Type	No. of PWAs Manufactured	No. of Control PWAs	No. of Assemblies Returned	Number of Failures	Number of Failed ICs *			Number of Failure Reports Missing **
						TOTAL	METERED	NOT METERED	
1	Mem. I/F	117	14	13	0	0	0	0	1
2	ALU	415	56	86	49	45	7	38	3
3	Panel I/F	492	73	69	31	27	8	19	2
4	Control 1	365	72	57	29	19	8	11	1
5	I/O TTY	248	60	84	32	26	10	16	4
6	SMI	545	73	31	14	14	5	9	0
7	Control 2	583	71	54	30	27	13	14	2
8	CR/LP	311	15	15	8	7	4	3	1
9	Transform	323	58	160	51	34	7	27	7
	TOTALS	3399	490	569	244	199	62	137	21

* IC Failures include both AC and DC and Infant Mortality failures.

** The three missing failure reports from the metered PWAs were exclude. since the probability of any one of the three containing a Non-Vendor A Novolac IC was 7%, for two to contain ICs was 0.5% and all three only 0.03%.

TABLE VIII

FAILURE SUMMARY OF PWAs NOT METERED

# of PWAs	Assembly	No. of ICs Replaced	No. of Non-ICs Replaced	Useful Life Failures SSI	MSI	LSI	# ICs used
295	C1	11	6	7	4	0	~~38464~~ 30985
512	C2	14	2	2	12	0	43520
472	SMI	9	0	2	7	0	48003
103	MI/F	0	0	0	0	0	~~13689~~ 12057
419	PI/F	19	0	4	15	0	62577
265	Tx	27	13	3	9	15	57825
359	ALU	38	4	2	16	20	34464
188	I/O TTY	16	6	4	12	0	19616
296	CR/LP	3	1	2	1	0	34040
	TOTALS	137	33	26	76	35	

FAILURE ANALYSIS

During this phase of the program there were a total of thirty-two ICs failure analyzed from metered PWAs including three infant mortality failures. Sixteen of these were A's devices of which three were CERDIP. Of the remaining sixteen failures analyzed, three could not be confirmed by CQL, eight were overstressed, four had oxide defects and one had a lifted bond.

Excluding the A's Novolac encapsulated failures the primary failure mechanism were overstress conditions which resulted from pin hole defects and mask defects, the most common non-package related defects found in bipolar ICs.

During the early manufacturing phase of the program A's Plastic encapsulated ICs did not have a protective passivation over the die. This lack of die protection was initially discovered via observing numerous failures during the qualification phase of this program. For this phase, of the thirteen (13) A's Novolac devices analyzed at CQL eleven did not have passivation over the die. Nine of these devices were determined to be non-functional with metal corrosion being either the failure mechanism or in evidence. The tenth could not be verified as a failure by CQL and the eleventh had an overstress condition. Both of the A's passivated devices analyzed had an overstress condition. The remaining seven A's failures, which were not analyzed including 4 infant mortality failures, were of the same device types and date codes as those analyzed and found to be non-passivated (dated coded between 7350 and 7415).

The significance of this failure analysis is that for the vendors which supplied ICs encapsulated in Novolac and having a glass passivation over the die there were not any corrosion problems detected. Also, none of the failures exhibited any broken or stressed wires due to expansion/contraction properties of the various materials making up the package.

The apparent difference in ratio of failures from metered PWAs and PWAs not metered can be explained by the number of CERDIP devices being used and the

usage of A's die passivated circuits. That is, the majority of PWAs built after the metered PWAs were shipped were manufactured by Company 2 where the percentage of CERDIP circuits were less than 3% of the total as compared to 13% for the metered PWAs. Also, A's Novolac encapsulated circuits manfactured after mid-1975 were passivated thus removing the corrosion failure mechanism. * Taking these two factors into account the ratios of failed Novolac and CERDIP packaged ICs are reasonably proportionate for the metered and not metered PWAs.

That is, of the 27 Novolac Failures, out of 490 metered PWAs, 9 were non-A's failures and of the 89 failures for the 2909 PWAs not metered 60 were non-A's failures (see Appendix 1 Figure 1 for the distribution of A's failures by date code and metered/not metered PWAs). The ratio of non-A's Novolac failures to both metered PWAs and PWAs not metered is approximately 2%.

* Although A's stopped processing non-passivated wafers in mid-1975 their non-passivated wafer inventory resulted in some non-passivated die being packaged, date coded and shipped to customers, as lat as the fourth quarter of 1976.

FAILURE RATE PREDICTION

Observed

Of the 490 metered PWAs shipped during the period 1/1/75 through 3/1/76 one hundred and seventeen (117) meters were read between 8/1/77 and 1/31/78. The majority of these, 87, were read in the field by Customer Engineering between 10/1/77 and 1/15/78. The time from the remaining thirty was taken from in-house machines (10) and PWAs that had been returned to DSLD during this same period (20). This data along with readings from an additional one hundred and one metered PWAs that had been returned to DSLD prior to 8/1/77 were used as a basis from calculation the Novolac failure rate. The readings from these two hundred and eighteen PWAs accounted for 123,896,400 device hours being accumulated, exclusive of the package type. 568,332 device hours per FWA

The observed failure rates for Novolac and CERDIP are given in Table IX.

It can be seen in Table IX that Vendor A's Plastic encapsulated IC data was removed from the other vendors data in order to determine the failure rate of Novolac encapsulated ICs currently being manufactured (ICs with passivated die).

Calculated

The calculated failure rate was determined by making two assumptions concerning the remaining 272 metered PWAs. These assumptions were:

1. 30% of the PWAs are spares and therefore did not accumulate hours.

2. An average system installed PWA receives a minimum of 500 operation hours per month.

These assumptions are considered to be very conservative in that (1) of the 87 meters read by customer engineering only three were classified as spares (2) seventy of the 87 meters read by customer engineering had exceeded 10,000 hours (3) all ten meters read from DSLD in-house machines had exceeded 10,000 hours and (4) several special site monitoring programs performed by the DSLD QA Department over the last two years indicated that the average site, independent of the class of machine installed, received in excess of 500 hours of on time every month.

Based on these two assumptions a minimum of 396,632,400 operating hours were accumulated over the life of the program. Extracting CERDIP hours (13.1%) and A's Novolac hours (27.2%) 250,922,349 operating hours were accumulated on Novolac encapsulated ICs with a total of 9 failures occurring. This equates to a failure rate of 0.042 failures per 1 x 10^6 operating hours at a 60% confidence level (see Table IX).

1,458,244 devices/PWA

TABLE IX

IC FAILURE RATE CALCULATIONS

Observed	PACKAGE	DEVICE HOURS	NUMBER OF * FAILURES	FAILURE RATE 60% Confidence level (Failures per $1x10^6$ operating hrs)	
	NOVOLAC and CERDIP	123,896,400	32	0.3	.03%/1ktu hrs
	CERDIP ONLY	16,230,428	5	0.39	.039
	NOVOLAC ONLY	107,665,972	27	0.28	.028
	NOVOLAC-FSC ONLY	29,285,144	18	0.68	.068
	NOVOLAC-LESS FSC	78,380,828	9	0.13	.013
Calculated					
	NOVOLAC and CERDIP	396,632,400	32	0.086	.0086
	CERDIP ONLY	51,958,844	5	.125	.0125
	NOVOLAC ONLY	344,673,556	27	.084	.0084
	NOVOLAC-FSC ONLY	93,751,207	18	.21	.021
	NOVOLAC-LESS FSC	250,922,349	9	.042	.0042

* See Appendix I, Table III for the distribution by vendor and package type

APPENDIX I - TABLE I IC COUNT BY PWA TYPE

Assembly	PWA IC Count		Total
	Metered	Unmetered	
ALU	5,376	34,464	39,840
C1	7,350	30,985	38,335
C2	6,035	43,520	49,555
SMI	6,497	48,003	54,500
PI/F	10,731	62,577	73,308
CR/LP	1,725	34,040	35,765
I/O TTY	5,680	19,616	25,296
TX	6,090	57,825	63,915
MI/F	1,638	12,051	13,689
TOTAL	51,122	343,081	394,203

APPENDIX I - TABLE II

CONTROLLED PWA IC COUNT BY PWA TYPE AND MANUFACTURE

Assembly/Package	Vendor A	B	C	D	OTHERS	TOTAL
ALU						
Novo	1478	640	527	2194	105	4944
Card	306	8	0	26	1	431
Others	0	0	1	0	0	1
Control 1						
Novo	2309	472	795	2557	205	6338
Card	932	0	1	27	36	996
Others	13	0	2	0	1	16
Control 2						
Novo	1683	386	812	2343	127	5351
Card	620	0	1	40	16	677
Others	2	0	2	0	3	7
SMI						
Novo	1382	826	664	2470	153	5496
Card	974	0	0	17	7	998
Others	1	1	1	0	0	3
Panel I/F						
Novo	3022	1145	1913	2576	530	9186
Card	964	1	1	41	365	1382
Others	0	0	2	0	171	173
CR/LP						
Novo	434	173	173	545	226	1551
Card	144	11	0	0	0	155
Others	0	0	1	0	18	19
I/O TTY						
Novo	1402	616	597	1711	293	4699
Card	846	0	0	13	106	965
Others	3	0	0	0	13	16
Transform						
Novo	1452	1061	951	1744	98	5306
Card	682	1	0	16	1	700
Others	17	0	64	0	3	84
Memory I/F						
Novo	669	168	130	248	49	1264
Card	351	3	5	0	14	373
Others	1	0	0	0	0	1
TOTAL						
Novo	13912	5487	6562	16388	1786	44135
Card	5959	24	8	180	546	6667
Others	37	1	73	0	209	320
GRAND TOTAL	19850	5512	6643	16568	2541	51122

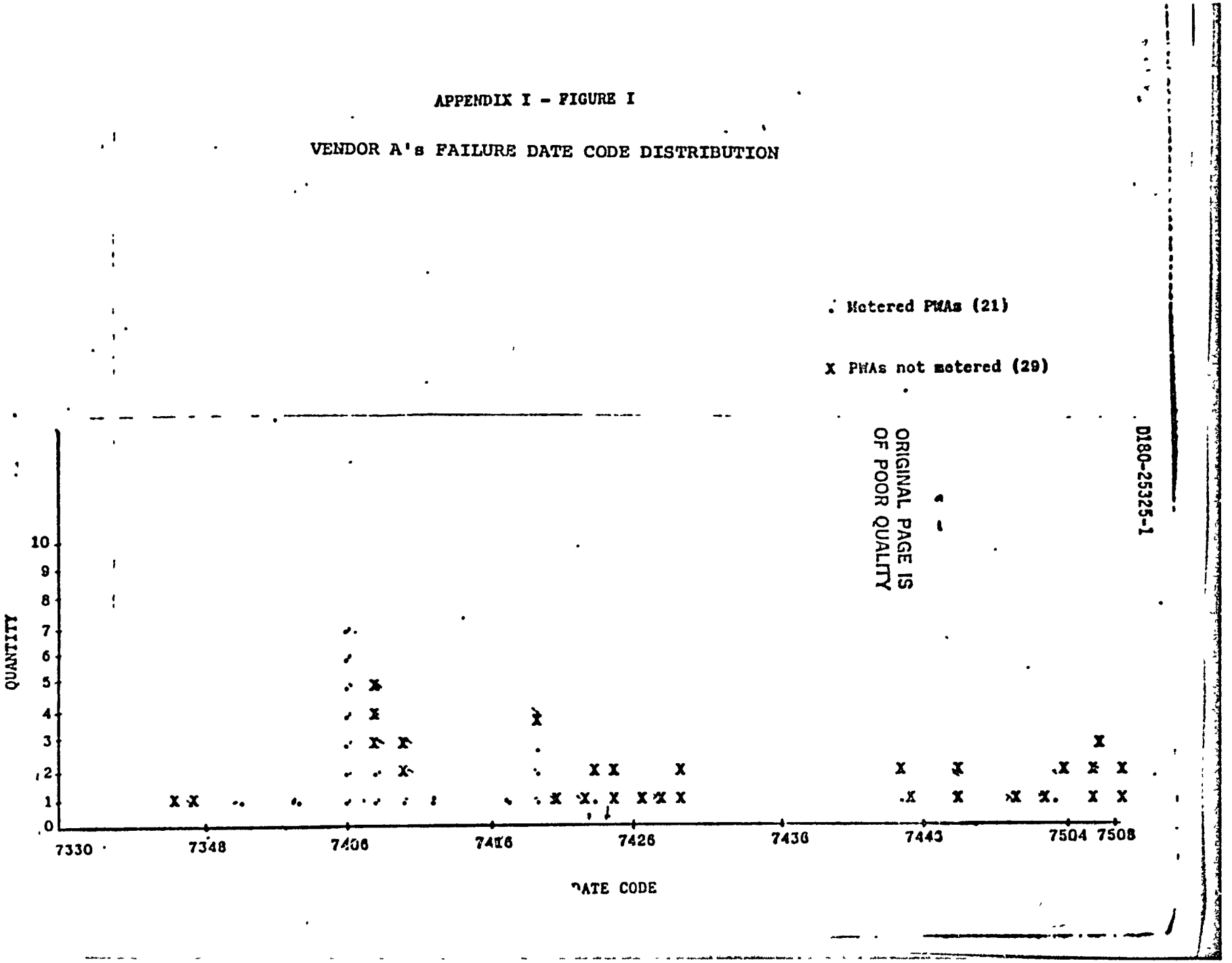
APPENDIX I - TABLE III

CONTROLLED PWA IC FAILURE COUNT BY PWA TYPE AND MANUFACTURE

Assembly/Package		Vendor A	B	C	D	OTHERS	TOTAL
ALU	Novo	0	1	0	0	1	1
	Card	0	0	0	1	0	1
	Others	0	0	0	0	0	1
Control 1							
	Novo	4	0	0	1	0	5
	Card	1	0	0	0	0	1
	Others	0	0	0	0	0	0
Control 2							
	Novo		0	0	0	0	1
	Card	1	0	0	0	0	1
	Others	0	0	0	1	0	1
SMI							
	Novo	0	1	0	1	0	2
	Card	1	0	0	0	0	1
	Others	0	0	0	0	0	0
Panel I/F							
	Novo	1	1	1	0	0	3
	Card	0	0	0	0	0	0
	Other	0	0	0	0	0	0
CR/LP							
	Novo	2	0	0	1	0	3
	Card	1	0	0	0	0	1
	Others	0	0	0	0	0	0
I/O TTY							
	Novo	6	0	0	2	0	8
	Card	0	0	0	0	0	0
	Others	0	0	0	0	0	0
Transform							
	Novo	3	0	0	1	0	4
	Card	0	0	0	0	0	0
	Others	0	0	0	0	0	0
Memory I/F							
	Novo	0	0	0	0	0	0
	Card	0	0	0	0	0	0
	Others	0	0	0	0	0	0
TOTAL	Novo	17	3	1	6	1	27
	Card	4	0	0	1	0	5
	Others	0	0	0	1	0	2
GRAND TOTAL		21	3	1	8	1	34

APPENDIX I - FIGURE I

VENDOR A's FAILURE DATE CODE DISTRIBUTION



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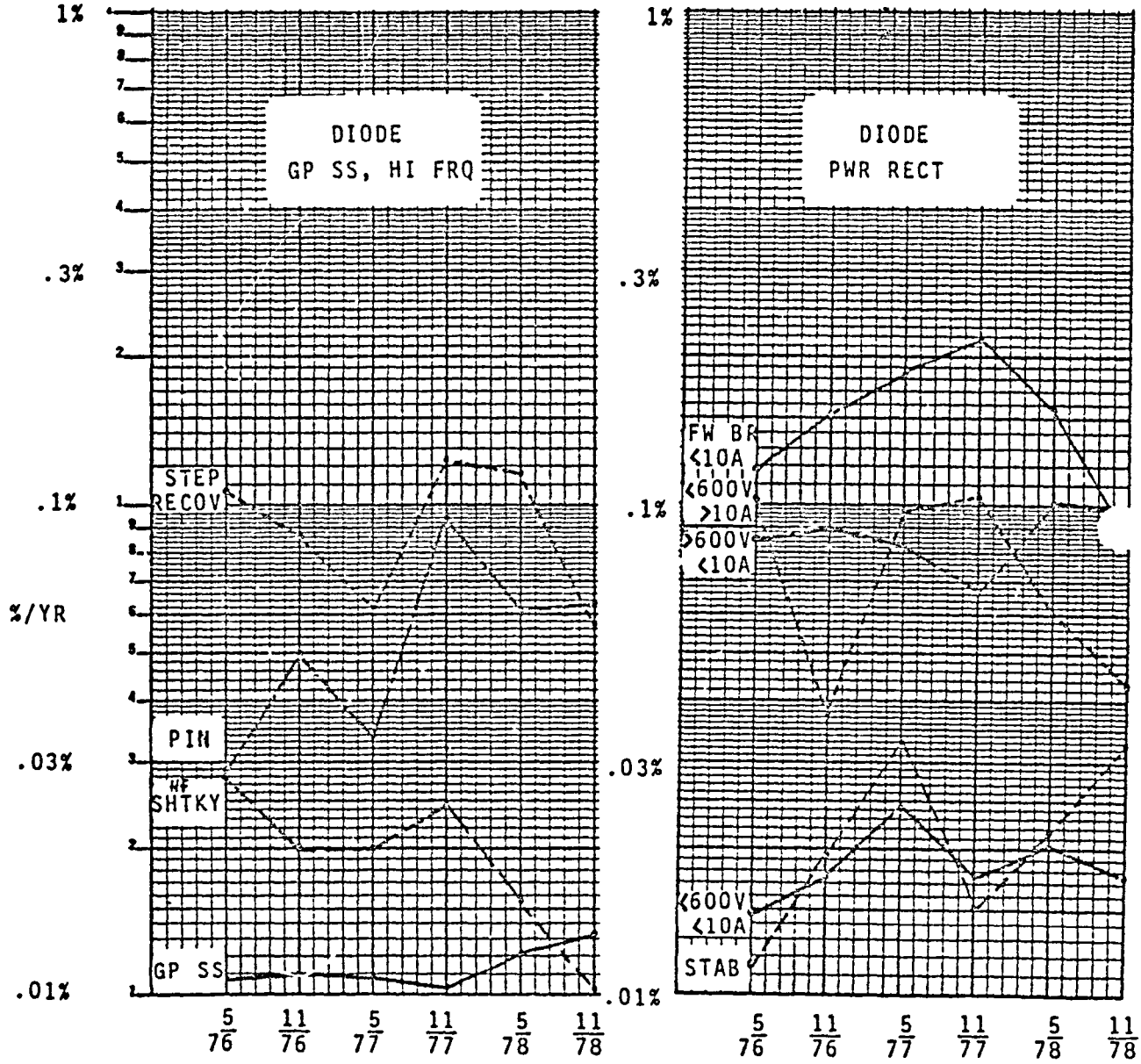
DEC 13 1978 DEC 31 1978

TYPE	CODE		(1976 parts) 6 mo fails f_6	5/77 parts/yr (21/011) W_{12}	%/yr	%/1Khr	1977 parts 6 mo fails f_6	11/77 parts/yr (24 hr) W_{12}	%/yr		6 mo fails f_6	5/78 parts/yr (24 hr) W_{12}	%/yr	whole year %/1Khr	1978 parts 6 mo fails (f_6)	4/78 parts/yr (24 hr) W_{12}	%/yr	%/1Khr	TREND
SS BIP-NPN-HERM	QSNJM		355	1,741,110	.1502	.025	359	1,28,130	.1104		374	1,257,652	.0550	.024	396	1,330,006	.0595	.025	FLAT
-PLASTIC	QSNJP		598	2,562,937	.1104	.017	551	2,274,133	.0383		532	2,332,236	.0382	.016	461	3,016,499	.0310	.013	IMPROVING
-PNP-HERM	QSPJM		315	955,215	.0659	.027	297	918,124	.0658		288	954,715	.0602	.026	280	910,122	.0595	.025	FLAT
-PLASTIC	QSPJP		550	2,071,550	.0541	.023	526	2,012,592	.0515		515	2,472,044	.0495	.021	460	2,249,321	.0415	.017	IMPROVING
SS JFET-N CHAN-HERM	QFNJM		94	270,721	.0670	.028	155	213,293	.1160		201	311,546	.1290	.051	182	374,403	.1056	.044	FLAT
-PLASTIC	QFNJP		173	177,322	.1951	.081	176	161,072	.2185		163	146,575	.1157	.086	152	162,576	.1814	.076	FLAT
-P CHAN-HERM	QFPJM		Ø	15,556	–		2	5567	.0719		Ø	5696	–	.030	Ø	6595	–	–	SMALL USE
-PLASTIC	QFPJP		27	71,842	.0755	.031	18	42,879	.0840		17	46,911	.0725	.033	23	46,147	.0997	.042	FLAT
PWR BIP-NPN-HERM (Fo.66)	(UT)		122	242,153	.1553	.065	172	245,748	.1100		218	250,057	.1744	.066	274	233,576	.2346	.098	FLAT
-PLASTIC	QPWPP		146	157,405	.1855	.077	132	152,134	.1735		114	165,355	.1379	.065	87	144,518	.1204	.050	IMPROVING
-PNP-HERM (Fo.66)	(UT)		32	57,161	.114	.047	73	59,165	.1154		38	61,147	.1184	.055	74	50,912	.1445	.060	FLAT
-PLASTIC	QSPPP		56	80,493	.1319	.058	40	79,17	.1014		28	86,416	.0648	.034	38	88,573	.0858	.036	IMPROVING
OP AMP-GP-HERM	JCLAM	✓	313	452,117	1221	.051	354	576,931	.1227	✓	372	641,853	.1159	.050	304	642,747	.0944	.039	FLAT
-PLASTIC	JCLAP	✓	57	72,158	.1635	.068	85	72,103	.1177	✓	54	71,130	.1518	.026	24	90,785	.0529	.022	VARIABLE
VOLT REG-FXD-HERM	(UT)	✓	70	23,724	.2141	.090	29	29,973	.1336	✓	30	36,968	.1622	.062	30	41,934	.1669	.070	FLAT
PLASTIC	(UT)	✓	39	31,310	.2210	.092	64	42,006	.3012	✓	48	50,189	.1913	.103	33	61,381	.1075	.045	IMPROVING
MECL MK-DIP PLASTIC	(UT)	✓	38	77,161	.0985	.041	40	75,098	.0588	✓	30	117,989	.0509	.029	51	204,775	.0498	.021	IMPROVING
-DIP CERAMIC	(UT)	✓	11	13,847	.1585	.066	9	13,878	.1924	✓	17	37,331	.0911	.038	35	83,576	.0837	.035	FLAT
CMOS SSI/MSI-DIP PLASTIC	(UT)	✓	191	225,022	.085	.029	71	259,218	.0702	✓	79	305,136	.0556	.025	99	342,618	(.0578)	.024	FLAT
-DIP CERAMIC	(UT)	✓	20	29,821	.1337	.056	23	40,835	.1126	✓	11	52,020	.0458	.033	25	63,797	.0737	.031	VARIABLE
VOLTREG-ADJ-HERM	(UT)	✓	147	100,274	.2532	.122	139	108,656	2559	✓	157	105,606	.2839	.112	118	58,082	.2407	.166	FLAT
-PLASTIC	(UT)	✓	20	5205	.7685	.320	20	5633	.7101	✓	21	6616	.7222	.298	16	9528	.3359	.140	Forecast 723 FC.

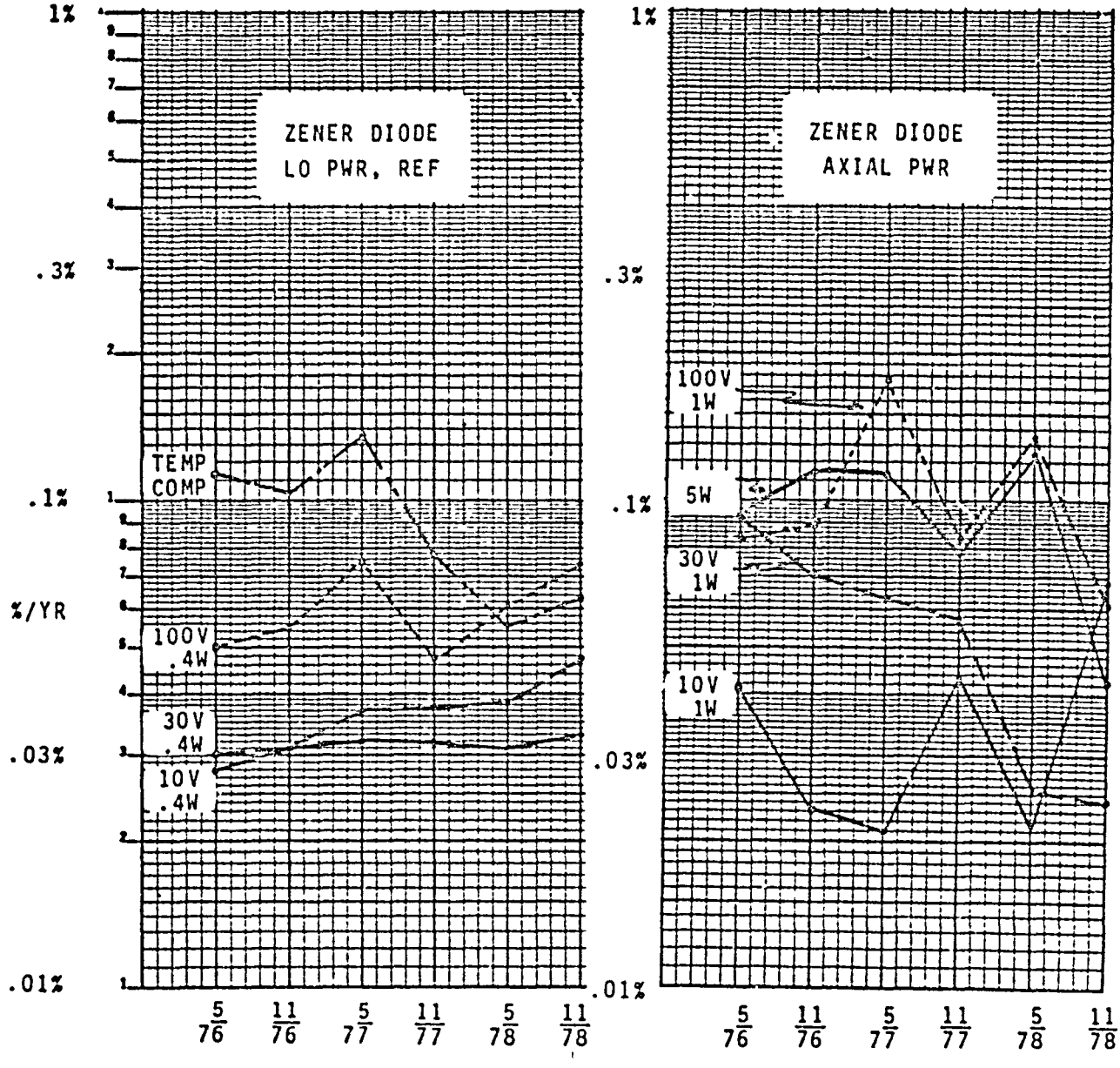
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



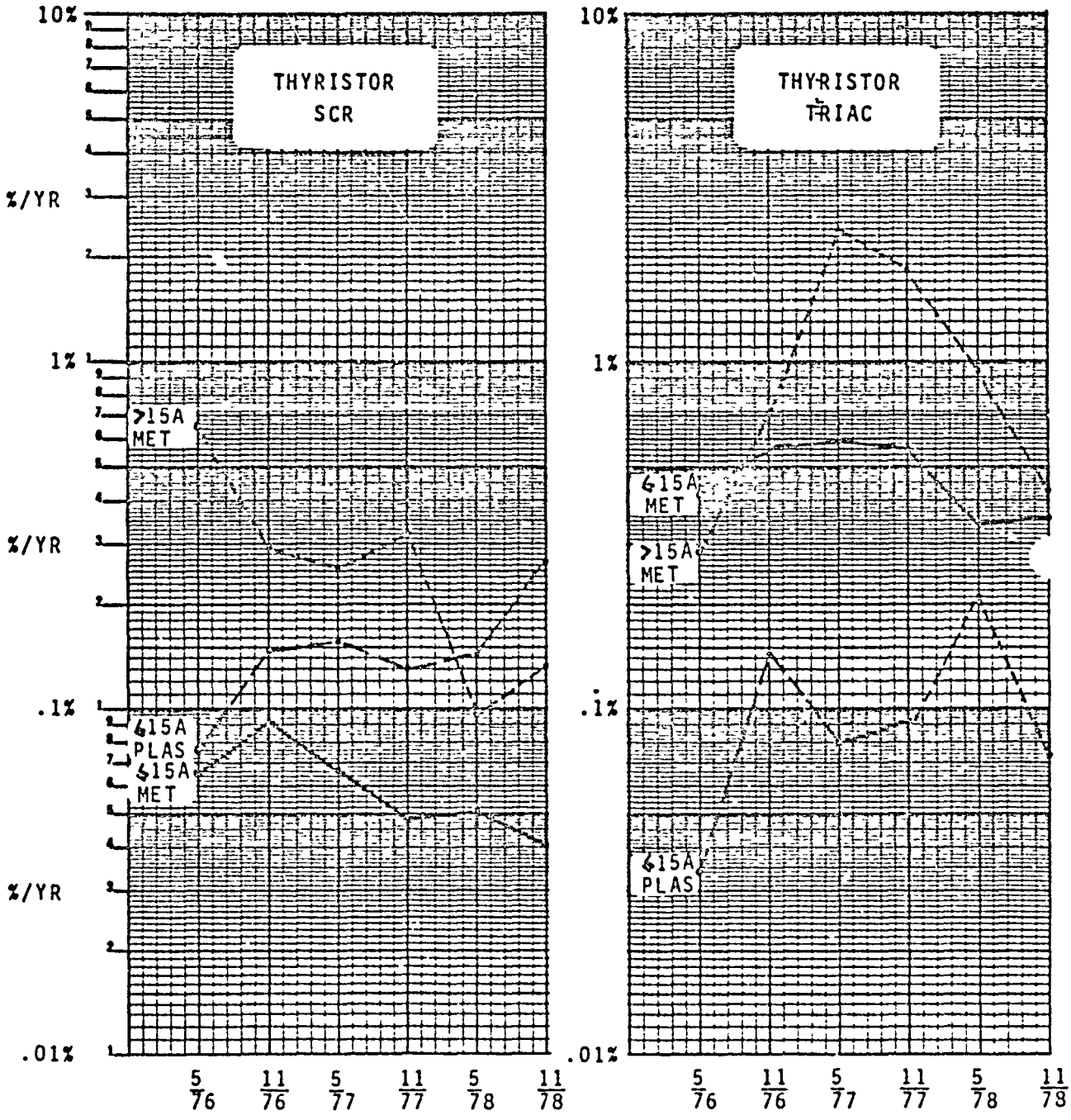
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



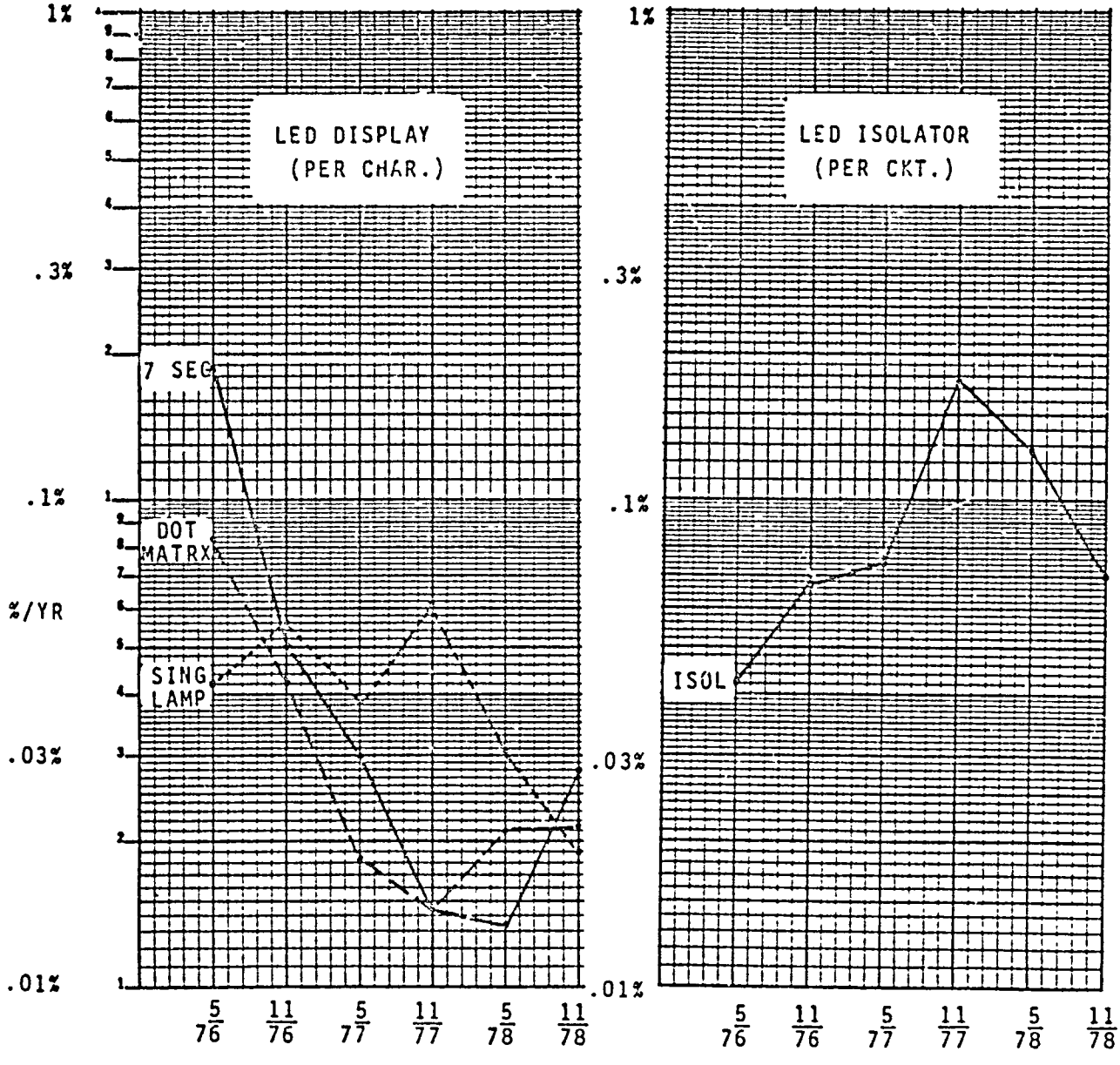
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



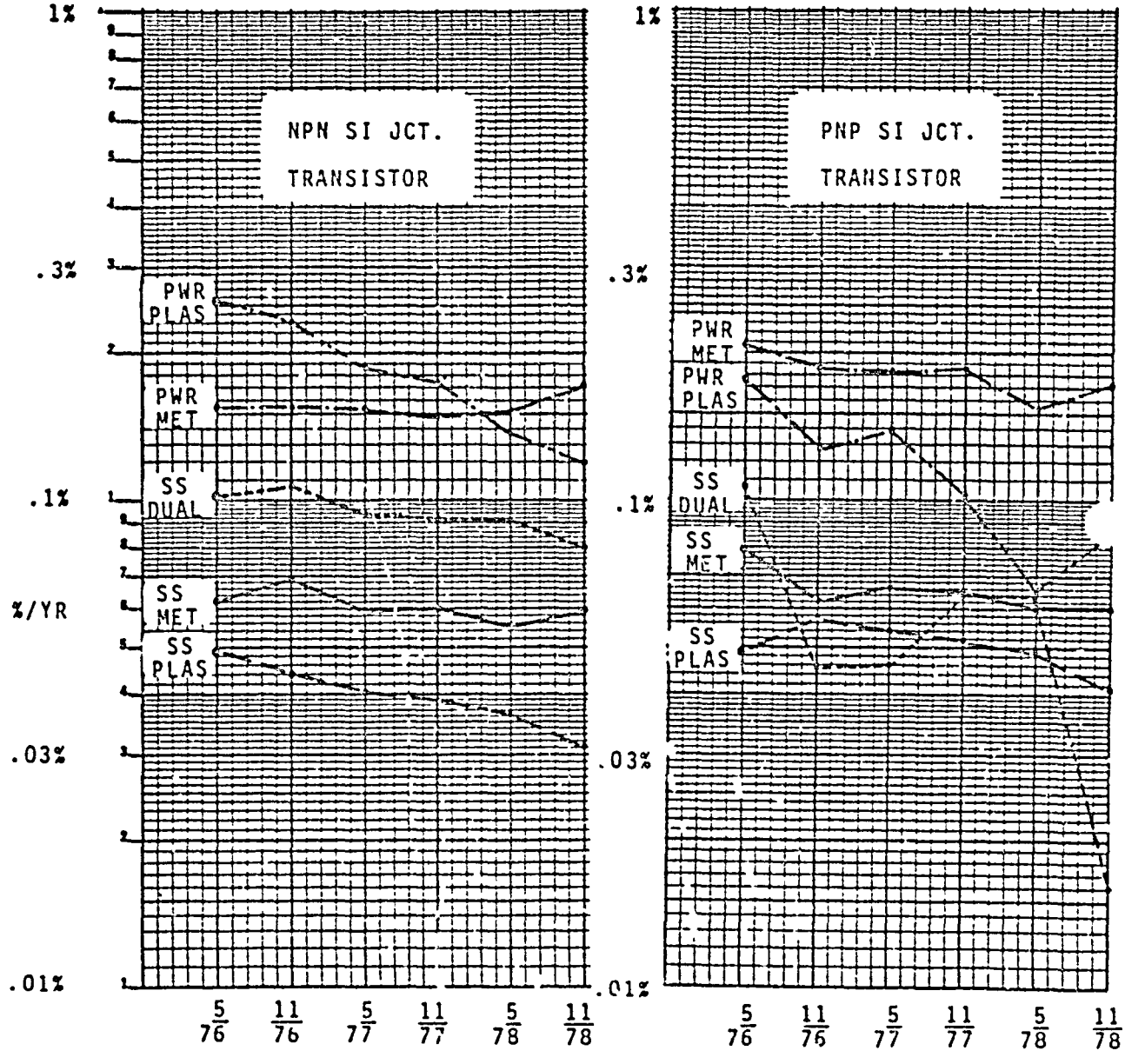
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



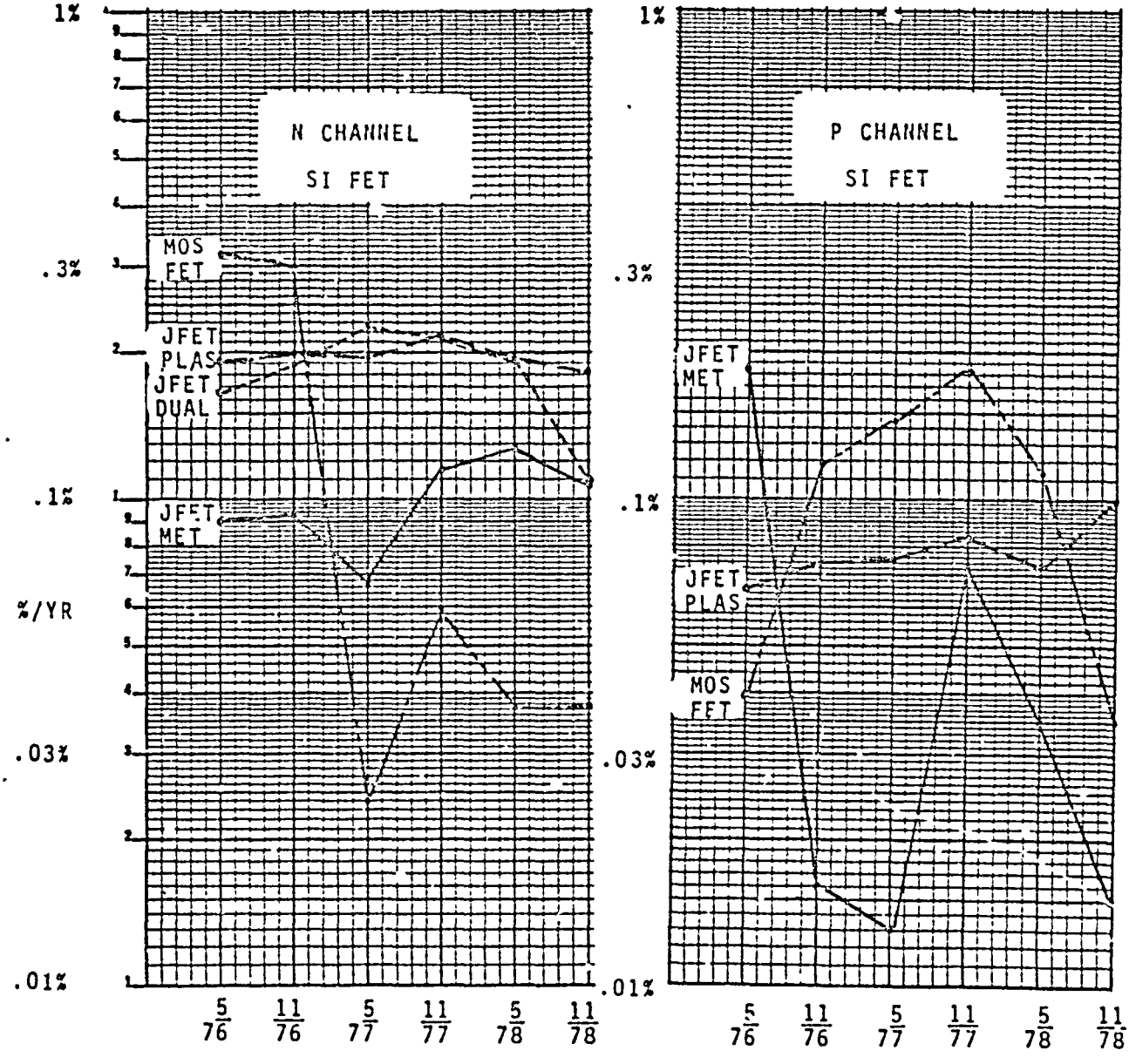
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



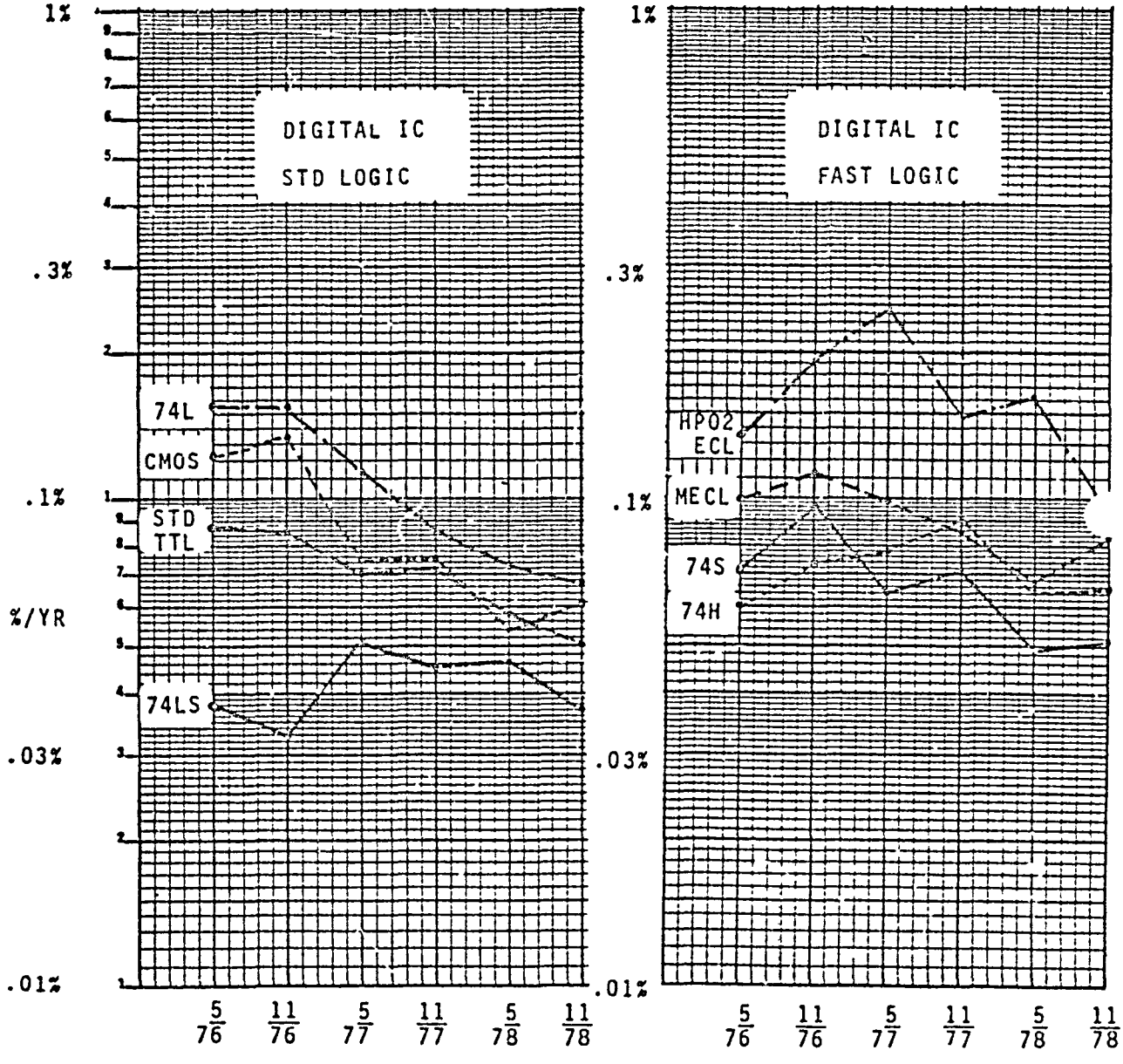
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



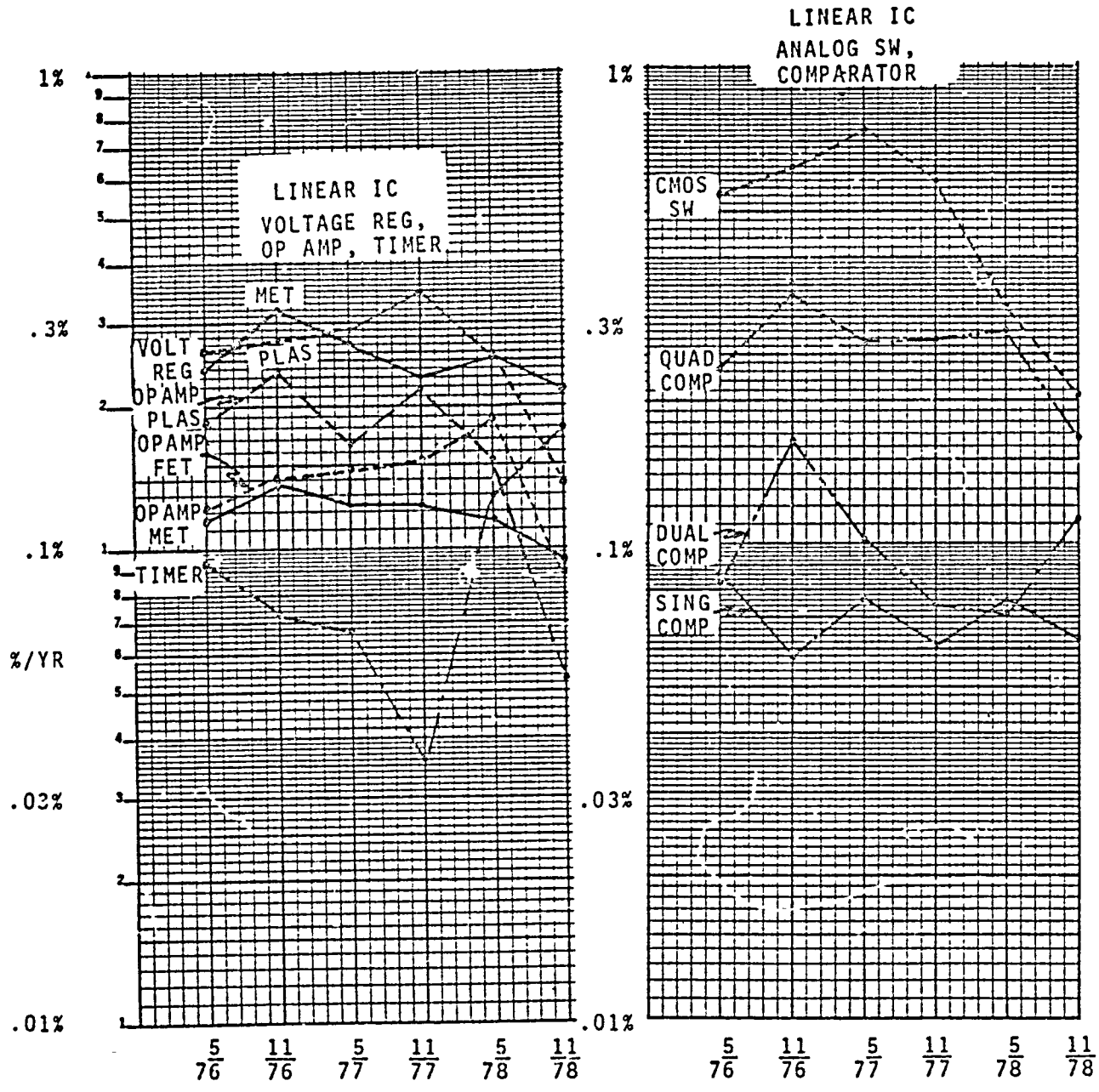
INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



INSTRUMENT GROUP WARRANTY REPLACEMENT RATES

%/YR (6 MONTH AVERAGES)



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DIGITAL FAILURE RATE SUMMARY

FIELD DATA – MERGED SUMMARY II

New Since MDR8 1977 parts

ENV.	OP. TYPE	SCREEN CLASS	GATE COMPLEX	JUNCT. TEMP. T_j	PACKAGE	TOTAL PART Hours	# FAILED	F/R %/1000hrs	
GM (7)	PMOS	N (13)	N.R.	N.R.	(PDIP)	240,000,000	67	.029	
"	TTL	N	(1-10)	(26-50)	HDIP	2,594,565	0		
"	ECL	N	(1-10)	(26-50)	HDIP	691,884	0		
"	TTL	N	(11-25)	(26-50)	HDIP	1,210,797	0		
"	TTL	N	(26-50)	(26-50)	HDIP	518,913	0		
All (3)	TTL	B-1 (5)	(1-10)	N.R.	HFPK	17,638,140	1		
"	TTL	B-1	(11-25)	N.R.	HFPK	3,222,358	0		
"	DTL	B-1	(1-10)	N.R.	HFPK	53,032	0		
"	HTTL	B-1	(1-10)	N.R.	HFPK	1,600,534	0		
"	HTTL	B-1	(11-25)	N.R.	HFPK	821,996	0		
"	TTL	B-1	(26-50)	N.R.	HFPK	1,697,024	0		
"	TTL	B-1	(51-75)	N.R.	HFPK	523,028	0		
"	TTL	B-2 to N (6)	(1-10)	N.R.	HDIP	5,645,374	4		
"	TTL	C-1 (10)	(51-75)	N.R.	HFPK	2,041,182	0		
"	ECL	B-2 to N (6)	(1-10)	N.R.	HFPK	4011	0		
"	TTL	B-2 to N	(11-25)	N.R.	HDIP	1,455,496	1		
"	TTL	B-2 to N	(26-50)	N.R.	HDIP	604,381	1		
"	PMOS	B-2 to N	(11-25)	N.R.	HDIP	16	0		
"	TTL	B-2 to N	(51-75)	N.R.	HDIP	719,482	0		
"	HTTL	B-2 to N	(11-25)	N.R.	HDIP	3477	0		
"	HTTL	B-2 to N	(1-10)	N.R.	HDIP	421,974	0		
"	DTL	B-2 to N	(1-10)	N.R.	HFPK	6536	0		

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			Complexity					FR %/1000hrs	
AIU (2)	TTL	C-1 (10)	(1-10)	N.R.	HFPK	14,991,352	3	1	
"	TTL	C-1	(11-25)	N.R.	HFPK	15,778,671	2		
"	DTL	C-1	(1-10)	N.R	HFPK	243,992	0		
"	HTTL	C-1	(1-10)	N.R.	HFPK	10,876,586	2		
"	TTL	C-1	(26-50)	N.R	HFPK	3,902,482	0		
"	ECL	C-1	(1-10)	N.R.	HFPK	230,000	2		
"	SUHL	C-1	(1-10)	N.R	HFPK	755,070	0		
"	SUHL	C-1	(11-25)	N.R.	HFPK	1,116,544	0		
"	TTL	C-1	(51-75)	N.R	HFPK	11,113,102	4		
"	HTTL	C-1	(11-25)	N.R	HFPK	915,785	0		
"	TTL	B-1	(1-10)	N.R.	HDIP	2,114,268	0		
"	TTL	B-1	(11-25)	N.R	HDIP	691,498	0		
"	TTL	B-1	(51-75)	N R	HDIP	27,106	0		
"	STTL	B-1	(1-10)	N.R	HDIP	135,530	0		
"	HTTL	B-1	(1-10)	N.R	HDIP	176,189	0		
"	TTL	B-1	(26-50)	N R	HDIP	121,977	0		
GB (FR)	STTL	(13) N	(11-25)	(26-50)	PDIP	6,131,898	4	.084%	STTL MSI
" "	TTL	13 N	(11-25)	(26-50)	PDIP	2,592,448	2	.15%	TTL MSI
" "	TTL	13 N	(26-50)	(51-75)	PDIP	78,600	1	2.6%	
" "	TTL	13 N	(1-10)	(26-50)	PDIP	3,453,912	0		SSI
" "	TTL	13 N	(51-75)	(26-50)	PDIP	627,792	0		
" "	TTL	3 X	(1-10)	(26-50)	PDIP	2,069,400	0		SSI

			Complexity						
GB (Fe.)	STTL	(12) X	(1-10)	(26-50)	PDIP	2,943,260	0		
" "	LSTTL	X	(1-10)	(26-50)	PDIP	851,652	0		
" "	HTTL	X	(11-25)	(26-50)	PDIP	153,068	1		
" "	TTL	X	(11-25)	(26-50)	PDIP	4,845,756	0		
" "	STTL	X	(11-25)	(26-50)	PDIP	2,957,524	1		
" "	STTL	12 X	(26-50)	(26-50)	PDIP	153,068	0		
" "	TTL	X	(51-75)	(26-50)	PDIP	153,068	0		
" "	CMOS	X	(76-100)	(26-50)	PDIP	153,068	0		
" "	TTL	X	(26-50)	(26-50)	PDIP	99,168	0		
" "	LSTTL	X	(11-25)	(26-50)	PDIP	6,975,840	0		
" "	TTL	X	(1-10)	(26-50)	HPPX	194,112	0		
" "	LSTTL	X	(26-50)	(26-50)	PDIP	10,800,000	0		
" "	LSTTL	X	(51-75)	(26-50)	PDIP	5,400,000	0		
" "	STTL	(13) N	(1-10)	(26-50)	PDIP	3,079,264	0		
" "	STTL	(13) N	(51-75)	(26-50)	PDIP	2,584,776	16		
" "	TTL	(13) N	(26-50)	(26-50)	PDIP	870,984	0		
" "	STTL	(13) N	(26-50)	(26-50)	PDIP	1,641,240	2		
" "	STTL	(12) N	(26-50)	(26-50)	HDIP	253,248	0		
" "	LSTTL	(12) N	(1-10)	(26-50)	PDIP	136,464	0		
" "	LSTTL	(12) N	(26-50)	(26-50)	PDIP	16,632	0		
		1							
GB (Pt.)	TTL	(12) N	(26-50)	(51-75)	PDIP	431,954,143	357		
" "	ECL	(12) N	(11-25)	(51-75)	PDIP	93,128,650	26		

					HP				
GB (R.R.)	LSTTL	N	(51-75)	(51-75)	PDIP	16,006,900	3		
" "	STTL	N	(26-50)	(51-75)	PDIP	11,115,000	5		
" "	STTL	N	(11-25)	(51-75)	HDIP	24,987,300	11		
" "	STTL	N	(51-75)	(51-75)	HDIP	24,434,800	18		
" "	ECL	N	(26-50)	(51-75)	HDIP	1,357,200	1		
" "	CMOS	N	(11-25)	(51-75)	PDIP	165,715,008	91		
" "	CMOS	N	(51-75)	(51-75)	PDIP	38,114,700	13		
" "	TTL	N	(76-100)	(51-75)	PDIP	40,950	0		
" "	ECL	N	(26-50)	(51-75)	PDIP	1,329,900	0		
" "	ECL	N	(11-25)	(51-75)	HDIP	5,654,350	8		
" "	ECL	N	(76-100)	(51-75)	HDIP	1,328,600	1		
" "	TTL	N	(11-25)	(51-75)	HDIP	2,002,500	4		
" "	CMOS	N	(76-100)	(51-75)	PDIP	40,199,250	18		
" "	TTL	N	(1-10)	(51-75)	HFPK	8,646,950	0		
" "	LTTL	N	(11-25)	(51-75)	HDIP	1,210,300	3		
" "	TTL	N	(76-100)	(51-75)	PDIP	291,200	0		
" "	CMOS	N	(26-50)	(51-75)	HDIP	8,835,450	8		
" "	STTL	N	(51-75)	(51-75)	PDIP	51,350	0		
" "	CMOS	N	(51-75)	(51-75)	HDIP	3,292,900	5		
" "	CMOS	N	(11-25)	(51-75)	HDIP	3,560,700	0		
" "	CMOS	N	(1-10)	(51-75)	HDIP	21,183,100	7		
" "	CMOS	N	(76-100)	(51-75)	HDIP	7,151,300	2		
" "	LSTTL	N	(1-10)	(51-75)	HDIP	479,700			

GB (e.e.)	DTL	N	(1-10)	(51-75)	PDIP	416,184,990	121		
" "	TTL	N	(1-10)	(51-75)	PDIP	2,998,930,972	663		
" "	TTL	N	(51-75)	(51-75)	PDIP	182,759,850	36		
" "	ECL	N	(1-10)	(51-75)	PDIP	403,783,750	131		
" "	TTL	N	(11-25)	(51-75)	PDIP	1,391,327,640	450		
" "	DTL	N	(1-10)	(51-75)	CAN	2,335,450	2		
" "	RTL	N	(1-10)	(51-75)	PDIP	10,515,050	11		
" "	HTTL	N	(1-10)	(51-75)	PDIP	283,656,650	68		
" "	HTTL	N	(11-25)	(51-75)	PDIP	57,300,100	10		
" "	TTL	N	(1-10)	(51-75)	HDIP	2,597,400	0		
" "	DTL	N	(11-25)	(51-75)	PDIP	1,320,150	1		
" "	LTTL	N	(11-25)	(51-75)	PDIP	601,932,224	330		
" "	LTTL	N	(26-50)	(51-75)	PDIP	276,692,850	102		
" "	LTTL	N	(1-10)	(51-75)	PDIP	659,983,110	485		
" "	LTTL	N	(51-75)	(51-75)	PDIP	99,146,384	45		
" "	STTL	N	(11-25)	(51-75)	PDIP	212,173,000	100		
" "	STTL	N	(1-10)	(51-75)	PDIP	424,786,059	87		
" "	LSTTL	N	(11-25)	(51-75)	PDIP	367,637,460	48		
" "	CMOS	N	(26-50)	(51-75)	PDIP	110,892,400	68		
" "	LSTTL	N	(1-10)	(51-75)	PDIP	676,313,950	136		
" "	LSTTL	N	(26-50)	(51-75)	PDIP	158,319,850	44		
" "	CMOS	N	(1-10)	(51-75)	PDIP	320,400,750	137		
" "	ECL	N	(1-10)	(51-75)	HDIP	22,205,300	16		

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GBC (R.R.)	TTL	N	(1-10)	(26-50)	PDIP	101,744,000	66		
" "	LTTL	N	(1-10)	(26-50)	PDIP	162,792,000	151		
" "	LTTL	N	(11-25)	(26-50)	PDIP	50,872,500	49		
" "	TTL	N	(26-50)	(26-50)	PDIP	10,174,500	7		
" "	LTTL	N	(26-50)	(26-50)	PDIP	20,349,000	4		
AI (1)	TTL	B-1 (5)	(11-25)	N.R.	HDIP	87,450	0		
"	TTL	B-1	(1-10)	N.R.	HFPK	573,300	0		
"	LTTL	B-1	(11-25)	N.R.	HDIP	7750	0		
"	TTL	B-1	(1-10)	N.R.	HDIP	69,750	0		
"	HTTL	B-1	(1-10)	N.R.	HDIP	3875	0		
"	HTTL	B-1	(11-25)	N.R.	HDIP	31,625	0		
"	TTL	B-1	(26-50)	N.R.	HDIP	19,500	0		
"	PTL	B-1	(11-25)	N.R.	HDIP	7750	0		
"	CMOS	B-1 or J8	(11-25)	N.R.	HDIP	105,840	0		
"	CMOS	B-1 or J8	(1-10)	N.R.	HDIP	211,680	0		
"	DTL	B-2 to N	(1-10)	N.R.	HFPK	219,624	0		
"	TTL	B-2 to N	(11-25)	N.R.	HDIP	44,863	0		
"	TTL	B-2 to N	(1-10)	N.R.	HFPK	5792	0		
"	DTL	B-2 to N	(26-50)	N.R.	HFPK	9030	0		
"	TTL	B-2 to N	(1-10)	N.R.	HDIP	82,371	0		
"	TTL	B-2 to N	(51-75)	N.R.	HFPK	7525	0		

AT	TTL	B-2 & N	(11-25)	N.R.	HFPK	5792	0		
GF (6)	CMOS	N	(1-10)	(26-50)	PDP	183,552	0		
"	TTL	TTL	(1-10)	(26-50)	HMP	49,353,810	1		
"	TTL	TTL	(11-25)	(26-50)	HDP	16,498,680	0		
"	TTL	B-1	(11-25)	(26-50)	HDP	50,743,834	1		
"	TTL	B-11	(51-75)	(26-50)	HDP	4,193,118	0		
"	TTL	TTL	(51-75)	(26-50)	HDP	1,536,084	0		
"	TTL	B-1	(1-10)	(26-50)	HDP	695,464	0		
"	TTL	B-1 & TTL	(1-10)	(N.R.)	HDP	998,089	0		
"	TTL	B-1 & TTL	(11-25)	(N.R.)	HDP	457,848	0		
"	TTL	B-1	(1-10)	(N.R.)	HDP	320,258	0		
"	HTL	B-1	(11-25)	(N.R.)	HDP	28,117	0		
"	TTL	B-1	(11-25)	N.R.	HDP	220,138	0		
"	STTL	B-1	(1-10)	N.E	HDP	167,740	0		
"	TTL	B-1 & TTL	(51-75)	N.E	HDP	67,096	0		
" (A)	HTL	B-1 & TTL (B)	(1-10)	N.R.	HDP	109,911	0		
"	STTL	B-1 & TTL	(1-10)	N.R.	HDP	364,873	0		
"	TTL	B-1	(51-75)	N.R.	HDP	24,047	0		
"	STTL	B-1 & TTL	(26-50)	N.R.	HDP	417,907	0		
"	STTL	B-1 & TTL	(11-25)	N.E	HDP	225,251	0		
"	TTL	B-1 & TTL	(26-50)	N R	HDP	178,602	0		

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GF (6)	STTL	B-1	(11-25)	N.R.	HDIP	148,892	0		
"	STTL	B-1 (5)	(26-50)	N.R	HDIP	25,241	0		
"	TTL	B-1	(26-50)	N.R.	HDIP	67,4 7	0		
"	STTL	N (13)	(11-25)	N.R.	HDIP	10,214	0		
"	HTTL	B-1	(1-10)	N.R.	HDIP	6710	0		
"	HTTL	B-1	(26-50)	N.R.	HDIP	97,448	0		
"	DTL	B-1	(1-10)	(26-50)	HDIP	14,359,486	0		
"	TTL	B-1	(26-50)	(51-75)	HDIP	6,357,862	0		
"	STTL	B-1	(1-10)	(26-50)	HDIP	1,286,580	0		
"	STTL	B-1	(11-25)	(26-50)	HDIP	444,224	0		
"	TTL	B-1	(51-75)	(51-75)	HDIP	15,961,758	0		
"	HTTL	B-1	(1-10)	(26-50)	HDIP	3,713,435	0		
"	HTTL	B-1	(11-25)	(26-50)	HDIP	83,292	0		
"	TTL	B-1	(26-50)	(26-50)	HDIP	3,525,756	0		
"	SUHL	B-1	(1-10)	(26-50)	HDIP	19,996,409	1		
"	SUHL	B-1	(11-25)	(26-50)	HDIP	7,989,384	0		
"	STTL	N	(1-10)	N.R	HDIP	320	0		
GT (12)	TTL	JB (14)	(1-10)	(26-50)	HDIP	12,451,276	0		
"	TTL	JB	(11-25)	(26-50)	HDIP	5,604,741	0		
"	TTL	B-1	(1-10)	(26-50)	HDIP	5,237,057	0		
"	HTTL	B-1	(1-10)	(26-50)	HDIP	352,785	0		

GT (10)	TTL	B-1 (5)	(11-25)	(26-50)	HDIP	3,899,946	0		
"	HTTL	B-1	(11-25)	(26-50)	HDIP	83,815	0		
"	LTTL	B-1	(11-25)	(26-50)	HDIP	1,237,272	0		
"	LTTL	JB	(1-10)	(26-50)	HDIP	2,908,402	0		
"	STTL	B-1	(1-10)	(26-50)	HDIP	2,316,291	0		
" (12)	STTL	B-1	(11-25)	(26-50)	HDIP	771,290	0		
"	STTL	B-1	(51-75)	(26-50)	HDIP	357,728	0		
"	LTTL	B-1	(26-50)	(26-50)	HDIP	2,410,031	0		
"	LTTL	B-1	(51-75)	(26-50)	HDIP	1,615,002	0		
"	TTL	B-1	(26-50)	(26-50)	HDIP	2,290,477	0		
"	TTL	B-1	(51-75)	(26-50)	HDIP	317,686	0		
"	TTL	JB	(26-50)	(26-50)	HDIP	1,361,406	0		
"	TTL	JB	(51-75)	(26-50)	HDIP	934,034	0		
"	LTTL	JB	(11-25)	(26-50)	HDIP	505,099	0		
"	LTTL	JB	(26-50)	(26-50)	HDIP	40,227	0		
"	TTL	JB	(26-50)	(26-50)	HFPK	36,564	0		

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A Comparative Evaluation of IC Packages in Commercial Real-Time Computer Terminals

C. M. Hall Jr., E. E. Shade, J. R. Shukis

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ASTC Descriptors: 831, 844, 833.

Key Words: Integrated Circuits, Failure Rates, Failure Modes, Components, Burn-in, Reliability.

Abstract

In the past few years there has been quite a bit of discussion over the relative merits of the new Epoxy B/Novolac IC packages versus the older style of plastics and Cerdip ceramics. An earlier paper by R. T. Sundus (Ref. 1) presented failure data on the old style plastic packages versus Cerdip ceramic packaged IC's and concluded that the old plastics were inadequate for current commercial real-time computer systems reliability requirements.

This paper describes a more recent program evaluating all three package types. Upon evaluating the data, the conclusion is presented that, whereas the reliability of the old style plastics was inadequate, the new Epoxy B/Novolac packages are equivalent to the standard Cerdips for bipolar IC's in commercial computer equipment.

Introduction

Early Plastics Problems

During 1971 and earlier, the plastic molding compounds utilized by the IC manufacturers were formulations of a silicone, phenolic or Epoxy A in which the glass transition temperatures were around 115°C or less. The predominant failure mechanism in these early plastic packages was open or intermittent bonds due to either poor bonding process control or to mechanical stress caused by significant differences in thermal coefficients of expansion of the various package constituents including the molding compounds.

Another major failure mode was package leaks due to poor adhesion of the plastics to the metal lead frame. These leaky packages resulted in failures due to die contamination, corrosion, metal migration, etc. This problem led to several IC process variations aimed at reducing the plastic permeability and plugging the "cracks" around the lead frames, such as backfilling or impregnating the molded package with hi-temperature wax compounds and/or coating the die with a drop of plastic after lead bonding and prior to encapsulation. None of these measures were adequately successful in making the old plastic parts as reliable as the Cerdip.

Vendor Package Improvements

During 1972, the IC manufacturers were developing the newer Epoxy B/Novolac plastic formulations which have glass transition temperatures around 150°C and higher. This higher glass transition temperature reduces internal mechanical stresses due to temperature change over the temperature range normally used for commercial equipment. In addition, the shrink factors of the Epoxy B Novolacs produce a much tighter grip on the metal lead frames, although it is still not a chemical or metallurgical bond, and these new formulations have a much lower permeability after molding.

The vendors also had made significant improvements in their lead frames, die attach and wire bonding materials, processes and process controls. Most of them had developed some form of glassivation to passivate the active surface of the die and protect it from the outside world. This technique also provided a degree of protection to the die from contaminants that might be in the plastic compound or that might enter the package by diffusion through the plastic case.

By 1972 and early 1973, all major IC manufacturers were utilizing these newer plastics to some degree and were extolling the advantages of Epoxy B/Novolac in eliminating the old problem of bond failures.

IC Package Evaluation Program

At this time we decided to implement a plastic IC evaluation program stressing the new Epoxy B/Novolac. The program had two main parts:

1. The Research & Engineering Reliability Group conducted a temperature cycle and 1,000 hour elevated temperature, high humidity, operating life test utilizing over 10,000 Epoxy B/Novolac devices from seven different vendors. The results of this work were reported by D. Lucas in April, 1974 (Ref.2) and they correlate well with the evaluation presented herein.

2. The Manufacturing R & QA Group performed an extensive evaluation program, utilizing production hardware and processes, which will be the main source of data for this paper.

Manufacturing Evaluation Plan

The following nine major steps define the evaluation plan developed by Manufacturing R & QA:

* Vendor Seminars and Plant Surveys
* User Plant Surveys
* Exhaustive Product Temperature Profile
* Verify Vendor Package Claims
* Build 3 Controlled Groups of Units
* Install all Units in Same Customer Store
* Provide "Total" Site Maintenance Support
* Record and Analyse Data & Failed Parts
* Implement Final Decisions

Preliminary Surveys

The product selected for evaluation consisted mainly of 7400 TTL and some off the shelf DTL circuits. A survey was conducted of the major suppliers' domestic plants and seminars were held to gain as much background as possible on package tests already conducted by various vendors. Similar plant visits and conferences were held with eight other major IC users who were successfully using substantial quantities of Epoxy B/Novolac IC's. These visits resulted in three conclusions.

1. We had to perform exhaustive product temperature profiles to assure that we had no severe hot spots.

2. We felt it desirable to verify the vendor's claims to a major reduction in bonding problems and thermal intermittents with the Epoxy B/Novolac packages

3. We wanted to perform a controlled build of a quantity of parts of sufficient terminals to evaluate alternative IC screening processes and the levels of reliability achieved.

The In Plant Evaluation Plan

The product temperature profiles indicated that there were only a couple of specific points of concern and these could be accommodated by special device selection, if necessary. It subsequently proved to be unnecessary.

Vendors' Claims Verification

To verify the vendors' claims to Epoxy B/Novolac package improvements, a thermal shock test was conducted as described in Figure 1. As a basis of comparison, 1500 devices of the old plastic and 1500 devices of the new Epoxy B Novolac (5 each from 3 vendors) were submitted to the test sequence

Devices that failed step 1 were replaced with other good devices of the same original lot so that 500 good pieces were in each group subjected to steps 2 through 5. The results are tabulated in Figure 2 and the conclusion is obvious, since the old plastics experienced 7.1% total failures apparently related to bonding problems, while the new Epoxy B/Novolacs experienced none.

Controlled Build Procedures

The controlled build of 60 208 terminals was then initiated as outlined in Figure 3. Cerdip ceramic IC's were to be used as the comparison base and were given no special processing after receipt from the vendor except the 100% screening tests shown in step 5 of Fig. 3, and a gross and fine leak test was performed on a sample from each lot for lot qualification. All plastic IC's, both old style and Epoxy B/Novolac, in each group were subjected to all of the tests described in Figure 3 for that group

The Green group process is the same as that which we were performing on all old style plastic production parts at the time of initiating this study. We felt the minimum reasonable process was a sample lot qualification for thermal intermittencies followed by 100% high temperature AC DC Functional and Parametric tests, as shown in the Yellow group. The Red group process fell between these extremes. The IC package type mix was predetermined for each group as shown in Figure 4. The purpose of these variations was to track the impact of certain changes on both product cost and performance

Many aspects of our process not related specifically to IC's were also studied and a good many interesting things were learned that are unrelated to this IC package evaluation.

Process Results

Both the IC's and printed wiring assemblies (PWA's) in each controlled group were color coded prior to beginning the assembly/test process. The three control groups were carefully tracked through each step of the manufacturing process and the in-plant data is summarized in Figure 5 "Incoming Inspection Test Results" and in Figure 6 "In Process Failures". In each case the data represents confirmed failed devices only. All invalid rejects, incorrect pulls by technicians, etc. have been purged from the data. All in-process rejects that retested good electrically were also thermal ramp tested to assure that a thermal intermittent did not exist.

It is interesting to note that the Total % Rejected in both Figure 5 and Figure 6 for Cerdip and Epoxy B/Novolac is approximately the same, whereas the old plastic Total % Rejected is from 1.5 to 3 times greater than the Cerdip.

The Field Site Evaluation Plan

It was our desire to install these controlled build terminals on a customer site where we could closely monitor their performance in actual use. We were very fortunate in that a major customer installation was scheduled to be made close to the point at the time these units would be ready to ship. Arrangements were made to do the site installation and provide all PWA repair services, etc. with factory technicians throughout the evaluation period. This assured continuity of maintenance support, tight control over failure data reporting and the capability to do detailed PWA and component failure analysis

As of July 15, 1974 this site had operated for 3,000 hours, which is approximately 42 weeks at 72 hours per week as shown in Figure 7. This gave us over 70 million part operating hours in the three controlled build IC groups.

Field Site Results

Every PWA failure that occurred on site was repaired in-plant and the IC failures confirmed. Figure 8 is a tabulation of the IC failure rates by control group and by IC package type. In each instance the Epoxy B/Novolac parts showed at least as good as the ceramics, while the old style hermetic plastics are approximately 3 times worse than the ceramics.

Component failure analysis has shown that several of the old style plastic failures are bonding intermittents, whereas none of the 3 Epoxy B/Novolac failures were bond problems and all three were hard failures. Elimination of the very last bond and excessive to bond intermittents is a major step in plastic IC improvements and a source is one of the IC vendors' claims for the Epoxy B/Novolac molding compounds.

Conclusions

From this study we concluded that the Epoxy B/Novolac molded IC's were the equivalent of Cerdip packaged devices in our application and that we could utilize them interchangeably without the use of expensive 100% burn-in, etc. Also in the Epoxy B/Novolac molding compounds reduce the incidence of bonding related problems, it is still possible to have a problem if the vendor's bonding machines get out of control

Since this is likely to be a lot cheaper problem, we implemented an incoming inspection process for Epoxy B/ Monolithic circuits that includes a thermal surprise temperature cycle (-55°C to +150°C, 10 cycles) followed by a thermal scan from 25°C to +125°C in a specially designed test set. See Figure 1 for a flow chart of the incoming inspection Epoxy B/ Monolithic IC Test Sequence that resulted from this study.

Acknowledgments

We would like to thank A. J. Kenney, Director of Plant Operations, for his assistance in implementing this study and frequent encouragement, and C. Maxwell, Manager Reliability & Data Analysis, Singer Business Machines, Albuquerque, for his assistance in performing the data analysis required in this study. Also we would like to express our appreciation to the major IC manufacturers for the time they devoted to seminars with us and test data they made available, and to the several other manufacturers who participated in informal discussions of this program during its development.

References

1. W. E. Sundin, "A Recommendation for Ceramic Over Plastic IC Packages in 1972 Real-Time Computer Systems", Proceedings of IEEE Reliability Physics Symposium, Las Vegas, Nevada. April 1972.

2. D. A. Lucas, "Epoxy (7400) Lead IC's - Final Summary", a Singer Business Machines internal report published April 24, 1974.

Biographies

Mailing address: C. W. Hall Jr.
Documation, Inc.
PO Box 1240
Melbourne, Fla. 32901

Mr. Hall received his BSEE degree from Carnegie Mellon University in 1951 and has been employed in a broad range of electronic equipment manufacturing during the past 20 years. He has over fifteen years experience in computer equipment Quality and Reliability Assurance with International Electric Corp., RCA Computer Systems Div., and Singer Business Machines Div. prior to his present assignment as Director Product Assurance, Documation, Inc. The work described in this paper was performed while he was Manager RFQA at Singer.

Mailing address: J. R. Shukis
Litton - Sweda Division
210 Welshpool Road
Lionville, Penna.

Mr. Shukis attended St. John Fisher College in Rochester New York, and has held a wide variety of engineering and management positions in manufacturing and quality assurance in the past 18 years. He has over 10 years in the military electronics industry with General Dynamics where his last position was Manager Field Vendor Assurance Engineering. He had 5 years experience with Sergeant Greenleaf as Manager Electronic Division responsible for manufacturing electronic components and relay switched remote control systems. Most recently he has over 4 years experience with Singer Business Machines in the manufacture of computer terminals as Manager Materials Dept. and as Manager Quality Assurance. He just recently assumed his current responsibilities as Plant Manager, Sweda, Lionville, Penna.

Mailing Address: E. E. Shade
National Cash Register Co.
PDS Supplier Quality Assurance
Dayton, Ohio

Mr. Shade has over 30 years experience in electronic systems equipment manufacture, maintenance, and operation. He has held approximately 10 years in Field Engineering on Radar and large scale computer systems with the US Army and RCA Service Co. Following this he spent 10 years with Honeywell, Inc. where he established a contract test equipment calibration/maintenance facility in Albuquerque, New Mexico and became Regional Manager of the Test Equipment Engineering Group. Over the past six years at Singer Business Machines, he has held several responsible positions, including Manager QA Systems & Projects, in which he was directly responsible for the coordination of this program, both in-house and on site, and it could not have been concluded as effectively without his dedication. He most recently assumed his new responsibilities in the Supplier Quality Assurance group of National Cash Register Corp., Dayton, Ohio.

1. DC Functional & Parametric @ 25°C & 70°C
2. Thermal Shock (Ice water/Boiling water) 10 cycles
3. Thermal Scan 25°C to 90°C
4. Stabilization Bake 96 Hrs @ 90°C
5. DC Functional & Parametrics @ 25°C & 70°C

Figure 1 Thermal Shock Qualification Test Sequence

Vendor	Epoxy B/No olac							Old Plastics						
	Qty Tested	Failure Data 25°C Qty	%	70°C Qty	%	Total Qty	%	Qty Tested	Failure Data 25°C Qty	%	70°C Qty	%	Total Qty	%
A	500	2	0.4	0	0	2	0.4	500	20	4.0	3	0.6	23	4.6
B	500	0	0	0	0	0	0	500	1	0.2	43	8.6	44	8.8
C	500	0	0	0	0	0	0	-	-	-	-	-	-	-
D	-	-	-	-	-	-	-	500	3	0.6	36	7.2	39	7.8
Total	1500	2	0.1	0	0	2	0.1	1500	24	1.6	82	5.5	106	7.1

Devices that failed at 25°C were not retested at 70°C.

The two vendor A Epoxy B/Novolac failures were not thermal intermittents. They were input leakage failures. All others were apparently bond related failures.

Figure 2. Thermal Shock Qualification Test Results

Process Steps	Process By Control Group 12 Brown	12 Red	17 Yellow
1	Visual	Visual	Visual
2	100% Temp Cycle -55°C/+125°C	100% Temp Cycle -55°C/+125°C	Sample Temp Cycle -55°C/+125°C
3	-	-	Sample Temp Scan
4	168 Hr Burn-in	120 Hr Burn-in	-
5	100% Functional & Parametric Test @ 25°C	100% Functional & Parametric Test @ 100°C	100% Functional & Parametric Test @ 70°C
6	PDA Funct'l Test Before Burn-in	-	-
7	72 Hr Post Burn-in		

Figure 3. 10 Process Variations

Package Type	Control Groups Brown		Yellow
CERDIP	64.2%	[illegible]	[illegible]
Old Plastic	21.2%	22.8%	[illegible]
[illegible]	11.1	[illegible]	[illegible]

Figure 4. Integrated Circuit [illegible]

Package Type	Brown			Red			Yellow			Total		
	Qty Tested	Qty Rej'd	%	Qty Tested	Qty Rej'd	%	Qty Tested	Qty Rej'd	%	Qty Tested	Qty Rej'd	%
Old Plastic	1670	15	0.9	1775	34	1.9	1425	18	1.3	4870	67	1.4
CERDIP	5091	53	1.04	3307	26	0.8	1575	13	0.83	9973	92	0.92
Epoxy B/ Novolac	1114	3	0.27	2793	19	0.7	4875	49	1.0	8782	71	0.81
Total	7875	71	0.9	7875	79	1.0	7875	80	1.0	23625	230	0.97

Figure 5 Incoming Inspection Test Results

Package Type	Brown			Red			Yellow			Total		
	Qty Used	Qty Rej	%	Qty Used	Qty Rej	%	Qty Used	Qty Rej	%	Qty Used	Qty Rej	%
Old Plastics	1670	26	1.55	1775	9	0.50	1425	23	1.6	4870	58	1.2
CERDIP	5091	24	0.47	3307	9	0.27	1575	10	0.63	9973	43	0.43
Epoxy B/	1114	6	0.53	2793	6	0.21	4875	17	0.34	8782	29	0.33
Total	7875	56	0.71	7875	24	0.30	7875	50	0.63	23625	130	0.55

These are confirmed failures - not process culls All failed parts that retested good at 70 C were also thermal ramped to assure lack of thermal intermittency.

Figure 6. In Process Failures

Package type	Qty IC's	Total Part Oper Hours
Old Plastic	4,870	14,610,000
CERDIP	9,973	29,919,000
Epoxy B/Novolac	8,782	26,340,000
Total	23,625	70,869,000

At the conclusion of the study this site (.5 terminals) had 3,000 hrs of operation. At 72 hrs/week = 41.7 weeks.

July 15 1974 Stopped
-42 wafers
July 15 1973 Installed
-1972 parts

Figure 7 Part Operating Hours Summary.

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Pkg Type	Control Number	Qty Failed	Total Population	% Failed	Total Part Operating Hours	Failure Rate
Old Plastic	Brown	5	1670	0.30	5,010,000	0.998x10⁻⁶
	Red	4	1775	0.23	5,325,000	0.751x10⁻⁶
	Yellow	3	1525	0.20	4,275,000	0.702x10⁻⁶
	Total	12	4970	0.25	14,610,000	0.821x10⁻⁶
CERDIP	Brown	3	5091	0.06	15,273,000	0.196x10⁻⁶
	Red	[illegible]	3307	[illegible]	9,921,000	0.403x10⁻⁶
	Yellow	[illegible]	1575	0.06	4,725,000	0.212x10⁻⁶
	Total	8	9973	0.08	29,919,000	0.267x10⁻⁶
Epoxy B Novolac	Brown	0	2114	0.00	6,342,000	0.000x10⁻⁶
	Red	[illegible]	2793	[illegible]	8,379,000	[illegible]
	Yellow	[illegible]	4875	[illegible]	14,625,000	[illegible]
	Total	3	9782	0.03	29,346,000	0.102x10⁻⁶

Figure 3. Field Failure Rate Breakdown

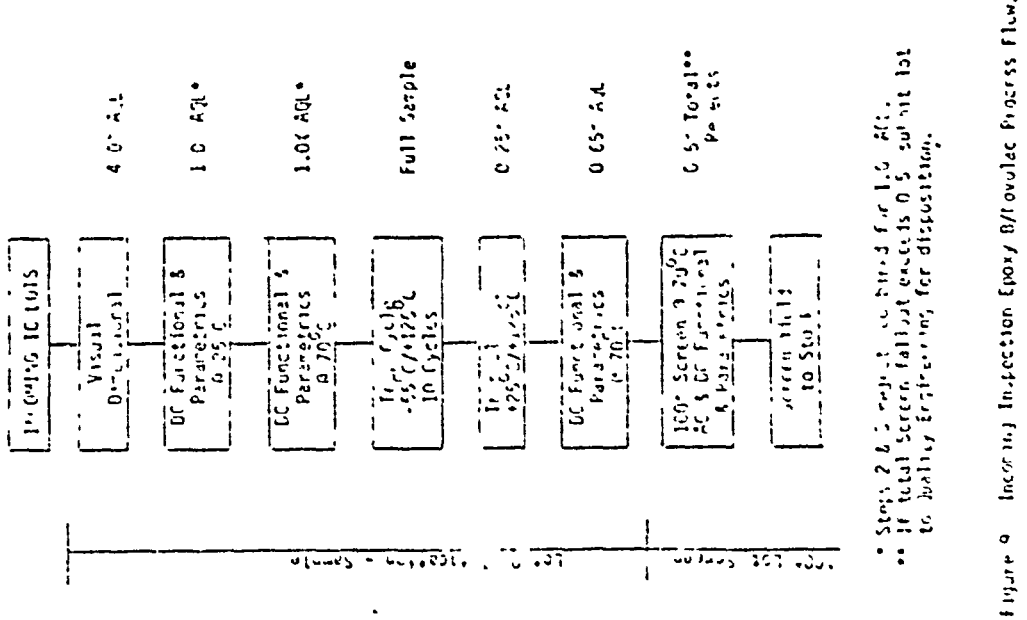

Figure 4 Incoming Inspection Epoxy B/Novolac Process Flow.

Appendix A.5 Manufacturer Information Request Letter

BOEING AEROSPACE COMPANY

P O Box 3999
Seattle, Washington 98124

M/S 88-43
A Division of The Boeing Company

April 6, 1979

Boeing Aerospace Company is performing a research contract for NASA/MSFC, Huntsville, Alabama, to determine the feasibility and guidelines involved in the use of plastic encapsulated semiconductors for space applications. As a result of the initial data gathering studies, it has been found that a number of users of molded devices are experiencing quite acceptable failure rates.

The next step is to determine the position of the semiconductor manufacturers in regard to reliability assurance through the application of low or minimal cost screening compatible with the low cost goals of plastic usage. Your assistance is requested to participate in technical discussions directed to answering three basic questions:

- What screens does your company feel are the optimum screens for such a Commercial High Reliability (CHR) program?
- What would be the cost adder for each of the suggested screens, based on a purchase lot size of 1000 parts?
- What predicted reliability number can be expected as a result of imposition of the suggested screens, and what is the predicted reliability number without any special screens beyond the normal quality assurance steps taken by your company?

Please keep in mind that this is only a research study and that no parts procurement is anticipated during this contract other than possibly small quantities of sample parts for stress testing.

There are some thirty categories of parts being included in this study as listed in Attachment 1. Discussions with your company would be concerned only with the parts that your company currently is manufacturing.

The base line for the high reliability screening approach at many manufacturers is the approach defined by such programs as the SUPR, PEP, MACH VI, B+, and A+ programs. However, these programs should not be considered as the only suitable approaches, in case there are other known screens that are less traditional but more effective and still low cost. The cost parameter may be put in perspective by indicating that it would be desirable to add only 5¢ to a 15¢ part, 50¢ to a $5 part, and $1 to a $20 part, for the performance of suitable reliability screening. Attachment 2 shows a tabulation of the type of information Boeing would like to discuss at your facility in the near future. The foregoing is intended to be a definition of the areas of discussion, rather than a strict constraint on the type of screening that would be acceptable.

I will be contacting you in the next few days to set up a possible time and place for conducting discussions of your company's ideas for the CHR (Commercial High Reliability) approach. If you have questions in the meantime, I can be reached at Boeing in Seattle on (206) 773-1074.

Thank you very much for your interest and participation.

Sincerely

BOEING AEROSPACE COMPANY

Donald D. Robinson

Donald D. Robinson

Attachments:

/cla

31 CATEGORIES OF PARTS TO BE CONSIDERED

- MICROCIRCUITS
  - BIPOLAR
    - SSI
      - LOGIC
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
      - LINEAR
        - AMPLIFIER
        - VOLTAGE REGULATOR
    - MSI
      - LOGIC
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
    - LSI
      - LOGIC - STTL
      - RAM
      - PROM
      - LINEAR
  - MOS
    - SSI - LOGIC - CMOS
    - MSI - LOGIC - PMOS
    - LSI
      - MICROPROCESSOR - NMOS
      - RAM
        - NMOS
        - PMOS
      - LOGIC - PMOS
      - ROM - PMOS
- TRANSISTORS
  - BIPOLAR
    - SMALL SIGNAL
      - NPN
      - PNP
    - POWER
      - NPN
      - PNP
  - FET
    - SMALL SIGNAL
      - N-CHANNEL
      - P-CHANNEL
- DIODES - SMALL SIGNAL AND ZENER
- SCR'S

POSSIBLE LOW COST SCREENING OPTIONS
FOR COMMERCIAL HIGH RELIALIBITY (CHR)

Category of Part _____

Screen	Conditions	Effectiveness	Cost per Part (Adder) (1000 Quantity)
High Temperature Storage	Number of Hours: Temperature:		
Temperature Cycling	Number of Cycles. Range of Temp:		
Burn In	Number of Hours: Temperature:		
100% Room Temperature Measurement	Functional: DC Parameters: AC Parameters:	Number of times performed: 1 | 2 | 3	
100% High Temperature Measurement	Temperature: Functional: DC Parameters: AC Parameters:	Number of times performed: 1 | 2 | 3	
High Voltage Stress	Overvoltage Ratio: Time of Application:		

APPENDIX B

NASA PARTS SELECTION CRITERIA FOR PLASTIC ENCAPSULATED SOLID-STATE DEVICES

Note: The document presented in this apperdix is intended to be a stand-alone document. It includes the information and selected charts from the body and appendices of this report.

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SELECTION CRITERIA FOR THE USE OF PLASTIC ENCAPSULATED SOLID-STATE DEVICES IN NASA APPLICATIONS

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SUMMARY

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PLASTIC ENCAPSULATED SEMICONDUCTORS SELECTION CRITERIA

FOR USE BY:
- PROGRAM MANAGERS
- PARIS ENGINEERS
- DESIGN ENGINEERS

ADDRESSES:
- COST
- RELIABILITY
- AVAILABILITY

COMPARES:
- COMMERCIAL PLASTIC ENCAPSULATED PARTS
- RELIABILITY-SCREENED PLASTIC ENCAPSULATED PARTS
- MIL-STD-975/MIL-SCREENED HERMETIC PARTS

PROGRAM MANAGER CONSIDERATIONS FOR PLASTIC ENCAPSULATED vs. HERMETIC PARTS

- WHAT TYPE OF PAYLOAD IS BEING DEVELOPED
- WHAT TYPE OF PARTS CAN MEET SYSTEM REQUIREMENTS
- ARE THERE COST CONSTRAINTS
- DOES SCHEDULE REQUIREMENTS FAVOR ONE PART OVER ANOTHER
- RELIABILITY REQUIREMENTS

DESIGN ENGINEERING CONSIDERATIONS FOR PLASTIC ENCAPSULATED VS. HERMETIC PARTS

- ARE PARTS ON PROJECT/NASA APPROVED PARTS LIST?
- WILL PART PARAMETERS MEET SYSTEM PERFORMANCE REQUIREMENTS?
- ARE PARTS AVAILABLE?
  - FOR BREADBOARDING
  - FOR PRODUCTION
  - FOR NEW TECHNOLOGY DEVICES
- ARE DERATING FACTORS CONSIDERED?
  - THERMAL - BASED ON SYSTEM DESIGN
  - VOLTAGE - BASED ON POWER SUPPLIES AND DEVICE CAPABILITIES
  - CURRENT - BASED ON POWER SUPPLY CAPABILITIES

PARTS ENGINEERING CONSIDERATIONS FOR PLASTIC VS HERMETIC PARTS

- RELIABILITY
  - FAILURE RATE FOR EACH SPECIFIC PART TYPE
  - SCREENING REQUIREMENTS FOR RELIABILITY ASSURANCE
    - * COMMERCIAL HI-REL SUCH AS SUPR II, A+, PEP
    - * NASA STANDARD FLOW
  - QUALIFICATION OF INCOMING LOTS
- AVAILABILITY
  - MULTIPLE SOURCES
  - SELECTION FROM HIGH PRODUCTION PART TYPES
  - ADVANCED TECHNOLOGY PARTS
- COST
  - PURCHASE COSTS
  - QUALIFICATION COSTS
  - VENDOR NEGOTIATIONS

SECTION 1.0

INTRODUCTION

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SELECTION CRITERIA FOR THE USE OF PLASTIC ENCAPSULATED SOLID-STATE DEVICES IN NASA APPLICATIONS

1.0 INTRODUCTION

Modern plastic encapsulated semiconductors have significant advantages for use in advanced electronic systems: cost, ruggedness, availability, and freedom from loose particles. Historically these advantages have been offset by a reputation of questionable reliability, but this picture has changed in recent years with the advent of novolac encapsulation compounds that have solved many of the problems previously reported. In addition, the manufacturers have addressed their processing problems to improve their yields, with the result that plastic encapsulated semiconductors now enjoy an improved reputation for reliability in the users community.

It is the intent of this document to define the parameters for making the necessary decisions for use or non-use of plastic encapsulated semiconductors in space or other NASA applications. Three levels of concern exist in this decision making process:

- The program manager
- The system designer
- The parts engineer

Each of the levels has differing concerns for the cost advantages, reliability risks and availability advantages involved in using plastic encapsulated semiconductors. Table 1-1 lists the major concerns for each of the above three levels. The factors involved in the decision making process are complex and continually changing due to the increased utilization of plastic parts by commercial users. It is the intent of this document to give the best visability on the current status of plastic device reliability/usage history and provide a selection guide for the safe utilization of plastic encapsulated semiconductors in selected NASA systems.

This data presented in this document have been obtained from actual field reliability data and vendor data. This document discusses the factual data, trade-off factors and risks, from the viewpoint of the three decision making levels. This document will be updated on a periodic basis to ensure that it is current with the present state-of-the-art.

As shown in Table 1-1, the major concerns of the three decision making levels are cost, reliability and availability. Before proceeding into the details of the decision making processes, a summary of the major factors involved in the decision as to whether or not to use plastic encapsulated parts will be given.

CONCERN	PROGRAM MANAGER	DESIGN ENGINEER	PARTS ENGINEER
RELIABILITY	o WHAT TYPE OF PAYLOAD WILL BE BUILT? o CAN SYSTEM REQUIREMENTS BE MET?	DERATING FACTORS TO BE INVOLVED. o THERMAL o VOLTAGE o CURRENT	PREDICTED RELIABILITY FOR EACH PARTICULAR DEVICE TYPE FROM EACH MANUFACTURER. o COMPARE TO HI-REL SUCH AS JAN OR CUSTOM SPEC. o QUALIFICATION REQUIREMENTS FOR EACH PART TYPE o RELIABILITY SCREENING REQUIREMENTS.
COST	LIFE CYCLE COSTS o PARTS PROCUREMENT COSTS o PARTS QUALIFICATION COST o RELIABILITY VERIFICATION TEST COSTS o PRE DELIVERY REPAIR COST o PRE LAUNCH REPAIR COSTS o LOGISTICS AND MAINTENANCE COSTS	DEVICE PERFORMANCE PARAMETERS OF COMMERCIAL VS MIL PARTS: WHAT IS COST OF SPECIFYING SPECIAL PARAMETER LIMITS?	WHAT IS TOTAL COST PER PART OF: o PARTS ENGINEERING o PARTS PROCUREMENT o PART QUALIFICATION o FAILURE ANALYSIS SUPPORT.
AVAILABILITY	SUPPORT OF SYSTEM DELIVERY SCHEDULES	WHAT NEW FUNCTIONS ARE AVAILABLE FOR DESIGN IN ACCEPTABLE SCHEDULE.	o MULTIPLE SOURCING REQUIREMENTS o NEW FUNCTIONS IN PLASTICS VS MIL o DELIVERY TIMES FOR SCREENED PARTS

TABLE 1-1 PLASTIC ENCAPSULATED SEMICONDUCTOR AREAS OF CONCERN

1.1 COST

Approximately 90% of all semiconductors are encapsulated in plastic packages, and this body of business has become the driving factor in the cost arena. The ceramic packaged parts are basically more expensive, with the additional cost ranging from pennies to dollars depending on the complexity. For the military qualified ceramic parts, the cost is even higher and the sales quantities are even lower. Table 1-2 summarizes the relative costs for two types of TTL microcircuits in DIP packages: an SSI device and MSI part. These are only two examples out of a large quantity of semiconductor devices. The figures for advanced LSI devices such as microprocessors and memories are even more dramatic for the differences between plastic and hermetic packages, but the data for in house screened parts are not yet available for these part types. However for the ultimate in low cost parts, the plastic encapsulated parts are seen to hold the edge. Details of the cost trade offs are presented in the subsequent sections to this document for each of the different categories of part types available ranging from transistors and diodes, to LSTTL SSI microcircuits to LSI microprocessors and memories.

1.2 RELIABILITY

The overriding concern in the use of plastic encapsulated semiconductors is the reliability question. Data gathered from users of commercial plastic semiconductors have now been tabulated and show that the reliability of plastic devices has improved so much that the technology is a viable competitor with hermetic devices. Figure 1-1 summarizes the most current (1977 and 1978) field usage failure rates for four important circuit types. Detailed plots of the failure rates versus time are presented in the appendix. The failure rates shown at the left of each box in Figure 1-1 are for parts with little or no screening for reliability improvement. Several sources of data have indicated that there is at least a 5:1 improvement in failure rate when reliability screening is invoked. This is important when one considers that the first column data in Figure 1-1 are mostly derived from warranty returns which represent infant mortality failures that are normally removed by burn-in.

SSI (54L/74L TYPE)	BASIC COST	ADDED FOR MFR IN-HOUSE REL SCREEN: TEMP CYCLE, BURN-IN 100% ELECTRICAL MEASUREMENT	TOTAL COST
PLASTIC (0-70°C)	.17	.25	.42
HERMETIC (0-70°C)	.19	.25	.44
HERMETIC (-55 - +125°C)	.30	$1.00 1/	$1.30
JAN CLASS B (-55 - +125°C)	$1.80	---	$1.80
PLASTIC (0-70°C)	.17	.39 2/	.56
MSI 54L/74L TYPE)			
PLASTIC (0-70°C)	$2.50	.35	$2.85
HERMETIC (0-70°C)	$3.00	.35	$3.35
HERMETIC (-55 - +125°C)	$4.00	$1.00 1/	$5.00
JAN CLASS B (-55°C - +125°C)	$6.00		$6.00
PLASTIC (0-70°C)	$2.50	.49 2/	$2.99

1/ 883B Screened

2/ Screened to a NASA Standard Flow See Table 1-5 for proposed NASA Standard Flow.

TABLE 1-2 RELATIVE COST FACTORS FOR BIPOLAR MICROCIRCUITS

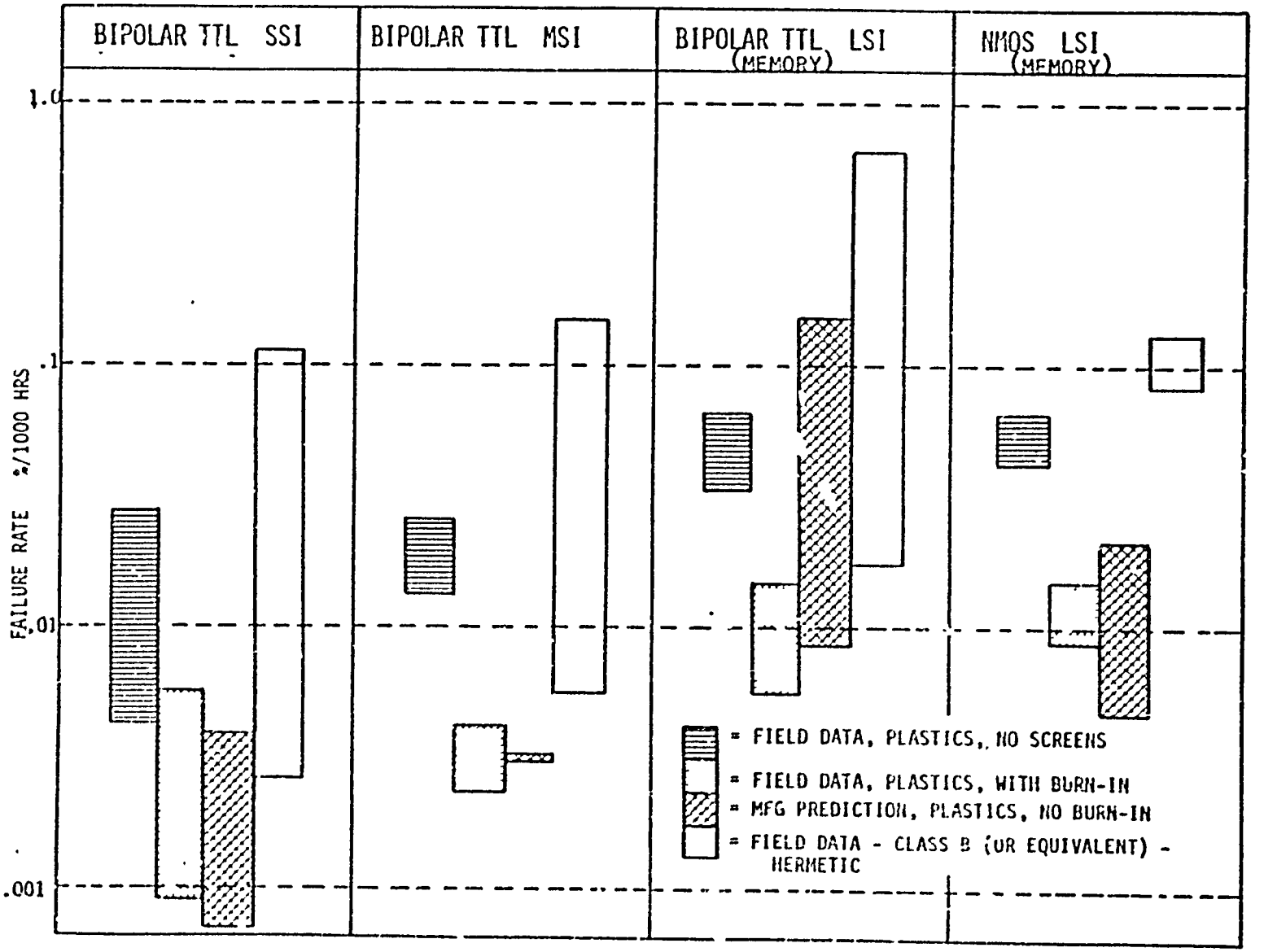


FIGURE 1-1 COMPARATIVE RELIABILITY OF PLASTIC ENCAPSULATED SEMICONDUCTORS

1.2 RELIABILITY (Continued)

In the second column of each box of Figure 1-1 is plotted the failure rate that would be expected if the parts had been burned-in. These plots are felt to be conservative since the 5:1 improvement factor is the minimum claimed by both users and manufacturers, with the actual range being as high as 15:1 improvement for some users.

The manufacturers perform a great deal of reliability testing and claim quite good reliability for their plastic encapsulated products. The third column in each box of Figure 1-1 shows the range of 55°C failure rates claimed by various manufacturers for each of the four product types. These manufacturers data are based on accelerated stress test data on non-burned-in parts. The discrepancy between the first column and the third column data can be explained by the fact that the field usage data are primarily based on warranty returns which are part removals but not necessarily failures. Actual failures probably constitute 1/2 to 1/3 of the total removals.

The fourth column in each box of Figure 1-1 shows the range of failure rates reported by Reliability Analysis Center for each of the product types as screened to the requirements of MIL-STD-883B, Class B (JAN equivalent devices, hermetic). The data are from the B-1 category of screening which means screened by the manufacturers in accordance with user specifications for parts comparable to JAN parts (as opposed to manufacturer in-house 883B equivalent screening, category B-2). As can be seen from the plots, the unscreened plastic parts are demonstrating very respectable reliability figures.

It must be pointed out that the plastic parts data were gathered from applications where the environment was benign, such as found in ground installation or test laboratories. However, the environment for space or other NASA applications can be considered as benign in terms of temperature variations and humidity, the two factors felt most severely to affect the reliability of plastic encapsulated semiconductors. This is verified by RAC which claims that satellite applications should have a π_E environmental failure rate multiplier of 0.2 while ground application have a π_E multiplier of 1.0.

It should be noted that similar data as shown in Figure 1-1 needs to be generated for linear and discrete devices. However, this data is not presently available and will be added to this document when it does become available.

1.2 RELIABILITY (Continued)

It has long been the contention of some sectors of the reliability and parts standardization community that the requirements of MIL-M-38510 for exhaustive qualification and testing or MIL-specification parts does not buy a much greater degree of reliability than merely performing 100% burn-in and electrical measurement at least 2 temperatures representing important operating areas. This seems to be borne out by the manufacturer-performed reliability screens available on commercial plastic encapsulated microcircuits. Many manufacturers advertise their screening program as being the answer to enhanced reliability of plastic encapsulated microcircuits. As seen by Table 1-3 there is little agreement between the manufacturers as to the test conditions to be used in performing the screens. The approach that is needed here is to generate a set of reliability-significant screens tailored to each of the different product types such that all manufacturers would be encouraged to perform the same screens on their products as every one else is performing, and perform these screens on a 100% basis.

Table 1-4 shows that the manufacturers do not even perform their advertised screens on all of their products, concentrating instead on the basic TTL oriented products. Most manufactures have expressed a willingness to perform some reasonable screens on even their advanced technology devices, and to this end a NASA standard flow for screening of plastic parts would be a significant contribution to the reliability control and improvement for plastic encapsulated parts.

The ingredients of the NASA Standard Flow are as shown in Table 1-5. It should be NASA policy that these standard screens would be performed on all plastic encapsulated microcircuits for all or any NASA contracted electronic designs. The benefit would be that the order quantities for parts with the special screening would be increased above the quantities resulting from individual contractors ordering quantities for just their own purposes.

PROGRAM / SCREEN	MANUFACTURER (1)	MANUFACTURER (2), LEVEL 3		MANUFACTURER (3) LEVEL A	MANUFACTURER (4) LEVEL B	MANUFACTURER (5) LEVEL 2	MANUFACTURER (6) LEVEL 5
		DIGITAL	LINEAR BI-MEM				
HIGH VOLTAGE STRESS AT WAFER PROBE			YES				
PRECAP VISUAL		YES			YES	YES	YES
TEMP CYCLE	10cy, -25/150°C	10cy, 0/100°C		5cy, 0/100°C air to air	15cy, 0/100°C Water shock	15cy 0/100°C Liquid shock	15cy 0/100°C Water shock
Continuity (I_{CC})		100°C					
Functional	100°C	100°C	25°C	25°C		25°C	25°C
DC PARAMETERS		100°C	25°C	25°C		25°C	25°C
BURN-IN	40hrs @ 145°C or 168hrs @ 125°C	21hrs @ 155°C		40hrs @ 150°C	24hrs @ 155°C	168hrs @ 125°C or 80hrs @ 150°C	168hrs @ 125°C
FUNCTIONAL	25°C	70°C	25°C	100°C, 25°C	100°C, 25°C	100°C	100°C
DC PARAMETERS	25°C	70°C	25°C	25°C	25°C	25°C	25°C

TABLE 1-3 COMMERCIAL HI-REL BASELINE SCREENS

PROGRAM	BIPOLAR SSI	LINEAR	BIPOLAR MSI	BIPOLAR LSI		CMOS	NMOS LSI		TRAN-SISTOR	DIODE
	TTL,LSTTL,ECL		TTL,LSTTL,ECL	RAM	LOGIC		μP	RAM		
MANUFACTURER (1)	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO
MANUFACTURER (2)	YES	YES	YES	NO	YES	--	NO	NO	NO	NO
MANUFACTURER (3)	YES	YES	YES	NO	YES	NO	NO	NO	LEVEL B ONLY	--
MANUFACTURER (4)	YES	YES	YES	NO	YES	--	NO	NO	--	--
MANUFACTURER (5)	YES	YES	YES	NO	NO	--	--	--	--	--
MANUFACTURER (6)	YES	YES	YES	YES	NO	YES	NO	YES	NO	NO
MANUFACTURER (7)	--	--	--	--	NO	--	NO	NO	--	--

YES MEANS YES, APPLIES TO THIS PRODUCT
NO MEANS DOES NOT APPLY TO THIS PRODUCT
-- MEANS NO PRODUCT IN THIS CATEGORY

TABLE 1-4

COMMERCIAL HI-RELIABILITY SCREENING PROGRAMS

TEMPERATURE CYCLING	30 CYCLES: $0^{o}C$ to $100^{o}C$, GAS TO GAS
100% FUNCTIONAL TEST	$100^{o}C$, $25^{o}C$
100% DC PARAMETERS	$100^{o}C$, $25^{o}C$
BURN-IN	168 HOURS AT $125^{o}C$ OR EQUIVALENT USING 1.0ev ACTIVATION ENERGY
100% FUNCTIONAL TEST PERFORMED TWICE (TWO PASSES)	$100^{o}C$ (RELAXED LIMITS) $25^{o}C$
100% DC PARAMETERS TEST PERFORMED TWICE (TWO PASSES)	$70^{o}C$ (RELAXED LIMITS) $25^{o}C$

TABLE 1-5

PROPOSED NASA STANDARD FLOW FOR
RELIABILITY SCREENING OF PLASTIC ENCAPSULATED MICROCIRCUITS

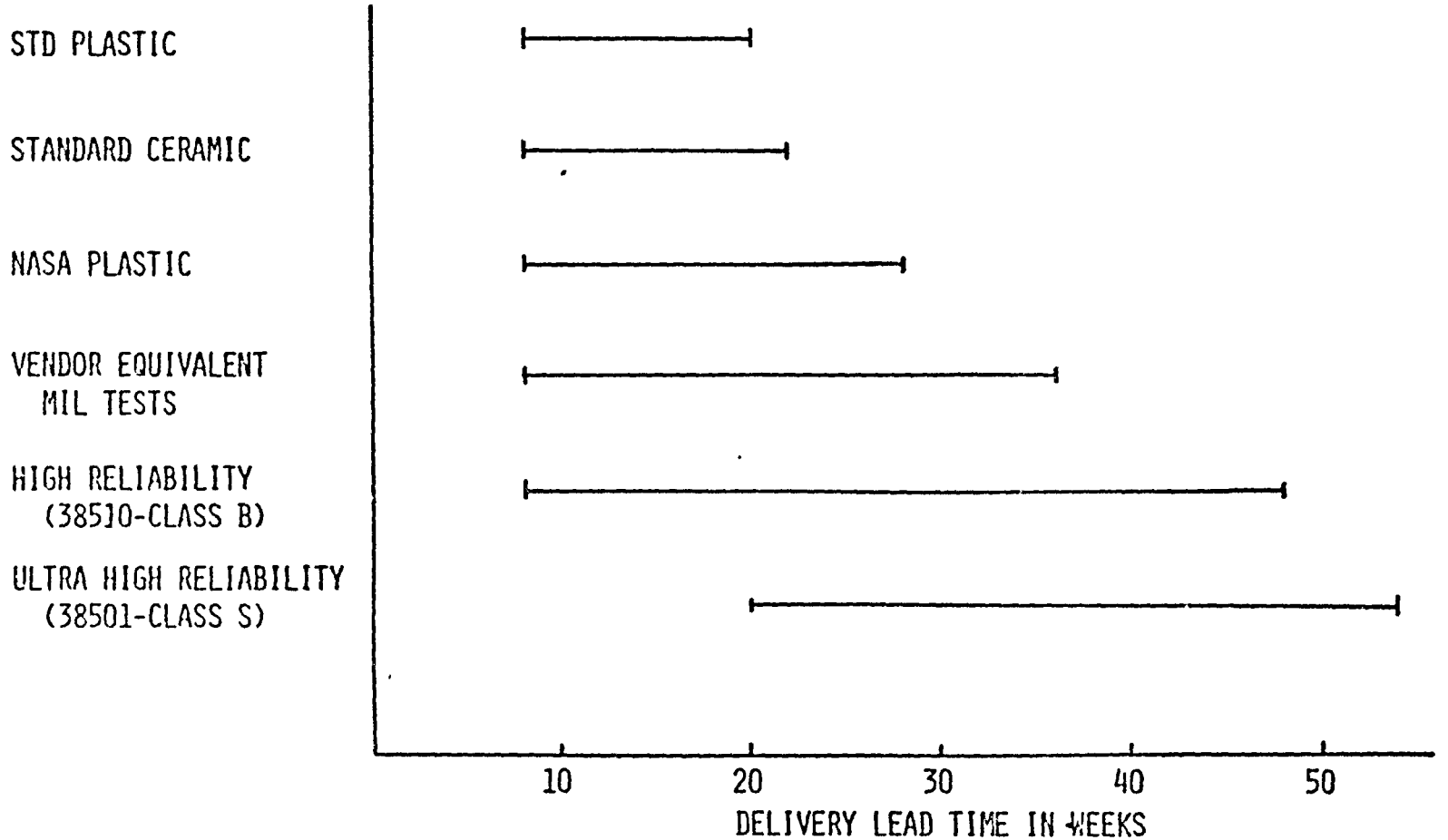
1.3 AVAILABILITY

The third factor of concern, that of availability, works in different ways for advanced LSI products compared to mature high production products. Generally speaking, new products of the LSI complexity are first introduced in hermetic packages and are not available in plastic until the high production process are well under control. When the plastic encapsulated devices are finally introduced, their prices are very low compared to the hermetic parts. Thus the availability of plastic in new technology devices is somewhat limited.

However, for the more commonplace high production mature products, plastic encapsulated parts are generally much more available than their hermetic counterparts as shown in Figure 1-2 Availability here translates into delivery times, with the plastic parts being available in a few weeks or even days, while the hermetic parts may require months. This is particular true for high reliability parts which must undergo reliability screening.

1.4 DEVICE TYPES ADDRESSED

The device types to be covered by this document are listed in Table 1-6.



NOTE 1: THIS CHART IS GENERALIZED TO SHOW BASIC TRENDS COVERING A WIDE VARIETY OF DEVICE TYPES. THE PARTS ENGINEER WILL HAVE CURRENT DATA ON SPECIFIC DEVICE TYPES.

NOTE 2: SEE TABLE 2-3 FOR MORE DETAIL.

FIGURE 1-2 GENERALIZED AVAILABILITY OF SEMICONDUCTOR DEVICES

- MICROCIRCUITS
  - Bipolar
    - SSI
      - Logic
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
      - Linear
        - Amplifier
        - Voltage Regulator
    - MSI
      - Logic
        - TTL
        - LSTTL
        - STTL
        - HTTL
        - ECL
    - LSI
      - Logic - STTL
      - RAM
      - PROM
      - Linear
  - MOS
    - SSI - Logic - CMOS
    - MSI - Logic - PMOS
    - LSI
      - Microprocessor - NMOS
      - RAM
        - NMOS
        - PMOS
      - Logic - PMOS
      - ROM - PMOS
- TRANSISTORS
  - Bipolar
    - Small Signal
      - NPN
      - PNP
    - Power
      - NPN
      - PNP
  - FET
    - Small Signal
      - N-Channel
      - P-Channel
- DIODES - Small Signal and Zener
- SCRs

TABLE 1-6: CATEGORIES OF PARTS COVERED BY THIS DOCUMENT

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SECTION 2.0

PROGRAM MANAGER CONSIDERATIONS

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2.0 PROGRAM MANAGER CONSIDERATIONS

The primary areas of concern for the program manager deal with the overall system performance and reliability requirements as well as program cost and schedule constraints. This section addresses the major decisions a program manager should make when considering whether or not plastic encapsulated devices should be used in selected applications for space systems.

The three main areas that need to be addressed by the program manager are:

- Reliability - Can the plastic devices meet payload reliability requirements?
- Availability - Do the schedule constraints of the program favor the generally more available plastic parts?
- Cost - What is the life cycle cost for using plastic parts as compared to hermetic or Mil-qualified parts?

Because of the continual changes in the status of plastic encapsulated semiconductors, no specific rules can be identified. What this section will provide is the identification of the means for obtaining sufficient data for making an optimized decision on the use of plastic encapsulated semiconductor devices.

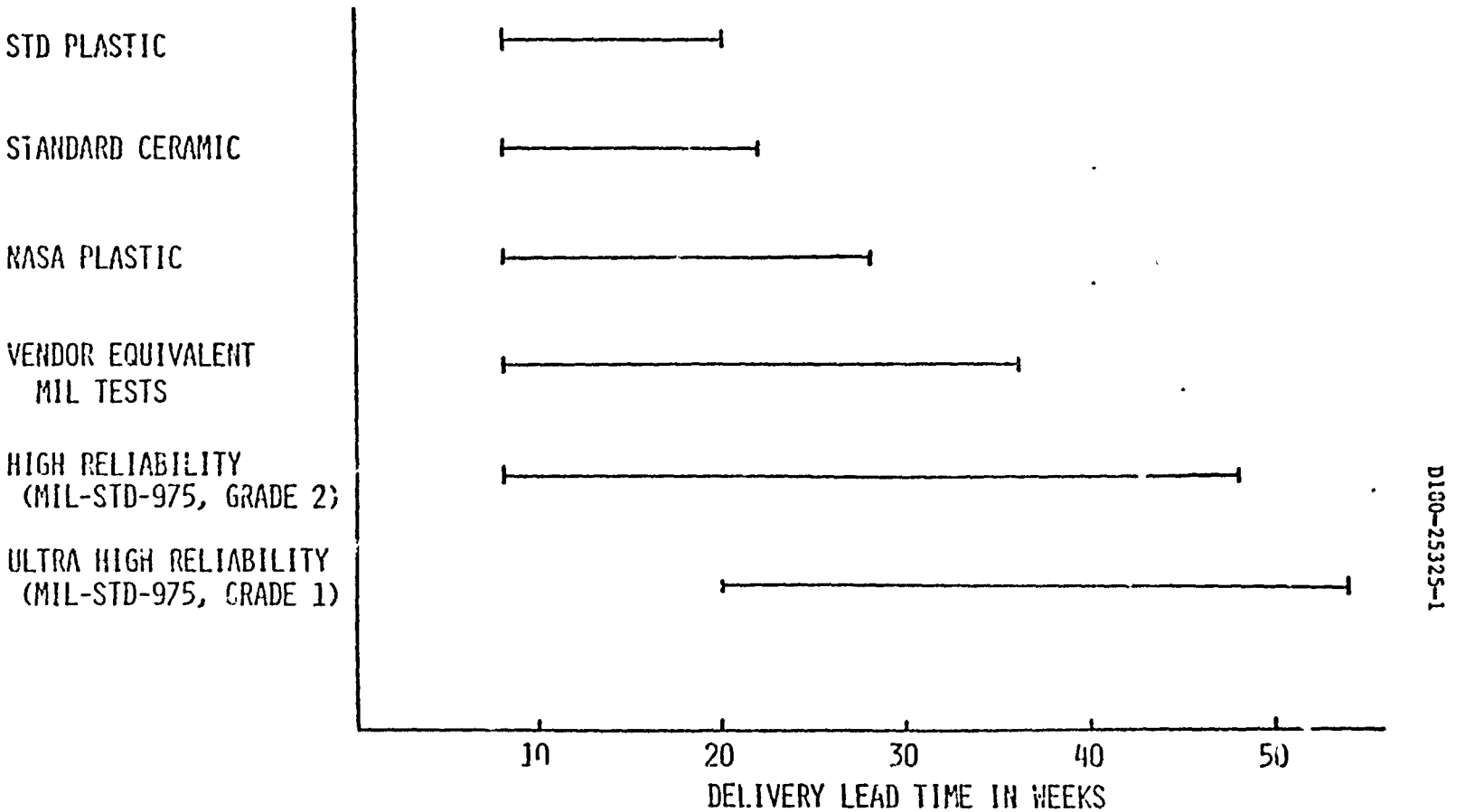
2.1 RELIABILITY

Data obtained from actual field data has shown that, when screened properly, plastic devices are as reliable as their military (extended temperature range) equivalent. However, the basic question to be answered is: How will plastic parts affect the MTBF of each individual subsystem.

Generalized criteria for using plastic parts are shown in Table 2-1. In high reliability/single point failure applications, the safest way to proceed is with fully qualified devices (MIL-STD-975, Grade 1 or 2, or equivalent). However, depending on the grade of device chosen, the lead time for obtaining the parts can be very long (Table 2-2). In cases where schedule constraints are the driving function, then the computation of the individual subsystem MTBF based upon plastic parts should be made. If the MTBF

CATEGORY	REQUIREMENT	SELECTION CRITERIA	POTENTIAL BENEFIT
UPPER STAGE PAYLOADS	• MISSION CRITICAL • SINGLE POINT FAILURE APPLICATION	MIL-STD-975, GRADE 1 OR EQUIVALENT	DEMONSTRATED RELIABILITY
	NON-SINGLE POINT FAILURE APPLICATIONS	MIL-STD-975, GRADE 2 OR EQUIVALENT	COST AVAILABILITY
		NASA PLASTIC ENCAPSULATED PARTS WITH DEMONSTRATED RELIABILITY	
DIRECTLY DEPLOYED PAYLOADS	• MISSION CRITICAL • SPF APPLICATION	MIL-STD-975, GRADE 1 OR EQUIVALENT	DEMONSTRATED RELIABILITY
	• NON-SPF APPLICATIONS • NONCRITICAL EQUIPMENT	MIL-STD-975, GRADE 2 OR EQUIVALENT	COST AVAILABILITY
		NASA PLASTIC ENCAPSULATED PARTS WITH DEMONSTRATED RELIABILITY	
ATTACHED: SCHEDULE CONSTRAINED OR CRITICAL OBJECTIVES	• MISSION CRITICAL • SPF APPLICATIONS	MIL-STD-975, GRADE 1 OR EQUIVALENT	DEMONSTRATED RELIABILITY
	• NON-SPF APPLICATIONS • NONCRITICAL EQUIPMENT	MIL-STD-975, GRADE 2 OR EQUIVALENT	COST AVAILABILITY
		NASA PLASTIC ENCAPSULATED PARTS WITH DEMONSTRATED RELIABILITY	
REFLYABLE ATTACHED: NOT SCHEDULE CONSTRAINED OR CRITICAL OBJECTIVES	NONE CRITICAL APPLICATIONS	NASA PLASTIC ENCAPSULATED DEVICES	COST AVAILABILITY

TABLE 2-1: SELECTION CRITERIA FOR PLASTIC ENCAPSULATED PARTS AS A FUNCTION OF APPLICATION



NOTE 1: THIS CHART IS GENERALIZED TO SHOW BASIC TRENDS COVERING A WIDE VARIETY OF DEVICE TYPES. THE PARTS ENGINEER WILL HAVE CURRENT DATA ON SPECIFIC DEVICE TYPES.

NOTE 2: SEE TABLE 2-3 FOR MORE DETAIL.

TABLE 2-2: GENERALIZED AVAILABILITY OF SEMICONDUCTOR DEVICES

2.1 RELIABILITY (Continued)

of the subsystem using plastic parts meets the requirements of the program, then these parts should be strongly considered for use. It should be noted that the project Parts Engineering organization has access to and can provide failure rate numbers for a wide variety of plastic parts in aiding the MTBF calculation. Field data has shown that the acceleration factors associated with MIL-HDBK-217C are extremely conservative and should not be used where actual field reliability data is known.

2.2 AVAILABILITY

The availability of general categories of plastic devices, as compared to military type devices, is shown in Table 2-3. The time shown in this chart includes release time, buyer time, transportation time, receiving tests, and shipment into stores. This chart shows that, in general, plastic devices are more readily available. If there is a tight schedule problem associated with a particular program, plastic parts can help alleviate part delivery problems.

The availability of plastic encapsulated devices varies from part type to part type. The Parts Engineering organization can give specific details on each part type. The general rule, however, is that plastic parts are more readily available.

2.3 COST

The cost benefits of using plastic encapsulated devices can be broken down into four main areas. These areas are:

- Part Procurement Costs
- Design Costs
- Manufacturing Costs
- Life Cycle Costs

Table 2-4 gives a comparison of potential cost savings associated with each area. In parts procurement, the data to-date indicate that there is an approximate 30% cost savings associated with the use of plastic encapsulated devices. Although the magnitude of the cost savings will vary from device type to device type, a cost savings is assured in the procurement cycle. The magnitude of the cost savings will depend upon the part type and part count in a particular subsystem. This figure can be obtained by contacting the Parts Engineering organization.

	DIGITAL	LINEAR	MEMORY	MICROPROCESSOR	TRANSISTOR DIODES & SCR
STANDARD PLASTIC	8-20 WEEKS	8-18 WEEKS	8-28 WEEKS	8-20 WEEKS	14-20 WEEKS
STANDARD CERAMIC	8-24	8-20	8-28	8-24	16-20
NASA PLASTIC	8-28	8-28	UNKNOWN	UNKNOWN	16-28
883B EQUIV.	8-36	8-24	8-42	8-30	N/A
CLASS B/GRADE 2	8-48	8-36	8-48	N/A	24-30
CLASS S/CUSTOM/ GRADE 1	20-56	20-52	20-52	N/A	20-52

TABLE 2-3: AVAILABILITY VERSUS DEVICE TYPE

COST AREA	COST BENEFIT/LIMITATION OF UTILIZING PLASTIC DEVICES
PROCUREMENT	APPROXIMATE 30% COST SAVINGS OVER COMPARABLY SCREENED HERMETIC DEVICES. (SCREENED PLASTIC VS. SCREENED HERMETIC)
DESIGN	- 10% MORE DEVICE FUNCTIONS (IN PLASTIC PACKAGES) RESULTS IN REDUCED PARTS COUNT - MAGNITUDE OF COST SAVINGS MUST BE MADE ON A CASE-BY-CASE BASIS
MANUFACTURING	NO SPECIFIC COST BENEFIT OF PLASTICS OVER CERAMICS
LIFE CYCLE	DEPENDENT ON MTBF (SEE FIGURE 2-1)

TABLE 2-4: COST SUMMARY OF PLASTIC PARTS

2.3 COST (Continued)

The cost savings associated with designing with plastic encapsulated parts will again vary based upon the design itself. There are approximately 10% more functions in plastic encapsulated parts than in hermetic devices. For a recent design (to be used experimentally in space) an A/D converter was needed. One plastic encapsulated device was selected for the function. To perform a similar function in hermetic packages would have required five integrated circuits and would have consumed three times as much power. Therefore, increased availability of functions (in plastic packages) allows for increased flexibility in developing a design. The magnitude of the cost savings can only be determined on a case-by-case basis.

In the area of manufacturing, there is no apparent cost benefits with the use of plastic encapsulated devices. The only possible benefit relates to Section 2.3, AVAILABILITY. With plastic encapsulated parts generally more available, they can better support manufacturing schedules. In the area of parts storage, handling, board insertion, solderability, cleaning and part marking, there is no clear cost benefit. Also, since field data has shown that plastic encapsulated devices are as reliable as their hermetic counterparts (screened to basically the same conditions), there is no substantial cost penality associated with the procurement and storage of plastic encapsulated devices to support manufacturing related failures.

The life cycle costs (LCC) for hardware equals the system acquisition cost plus the support costs. Figure 2-1 shows a typical life cycle cost for an arbitrary number of systems. It shows that the LCC varies as a function of MTBF. This figure is based in mathematics and verified by DoD field usage data (there is insufficient NASA data to-date to verify the curve for NASA applications). However, it shows the general relationship between acquisition costs, maintenance costs, and LCC.

When considering the use of plastic encapsulated parts, it will be necessary to determine the effect of these devices on LCC. This can be done by computing the MTBF of a particular subsystem based upon plastic encapsulated parts and MIL-grade hermetic devices. The difference in MTBF, in conjunction with data as shown in Figure 2-1, will indicate the potential cost savings/loss associated with plastic encapsulated devices. For example, if the MTBF comes out to be 800 hours for the MIL-grade parts and 700 hours for the plastic parts, there will be a negligible

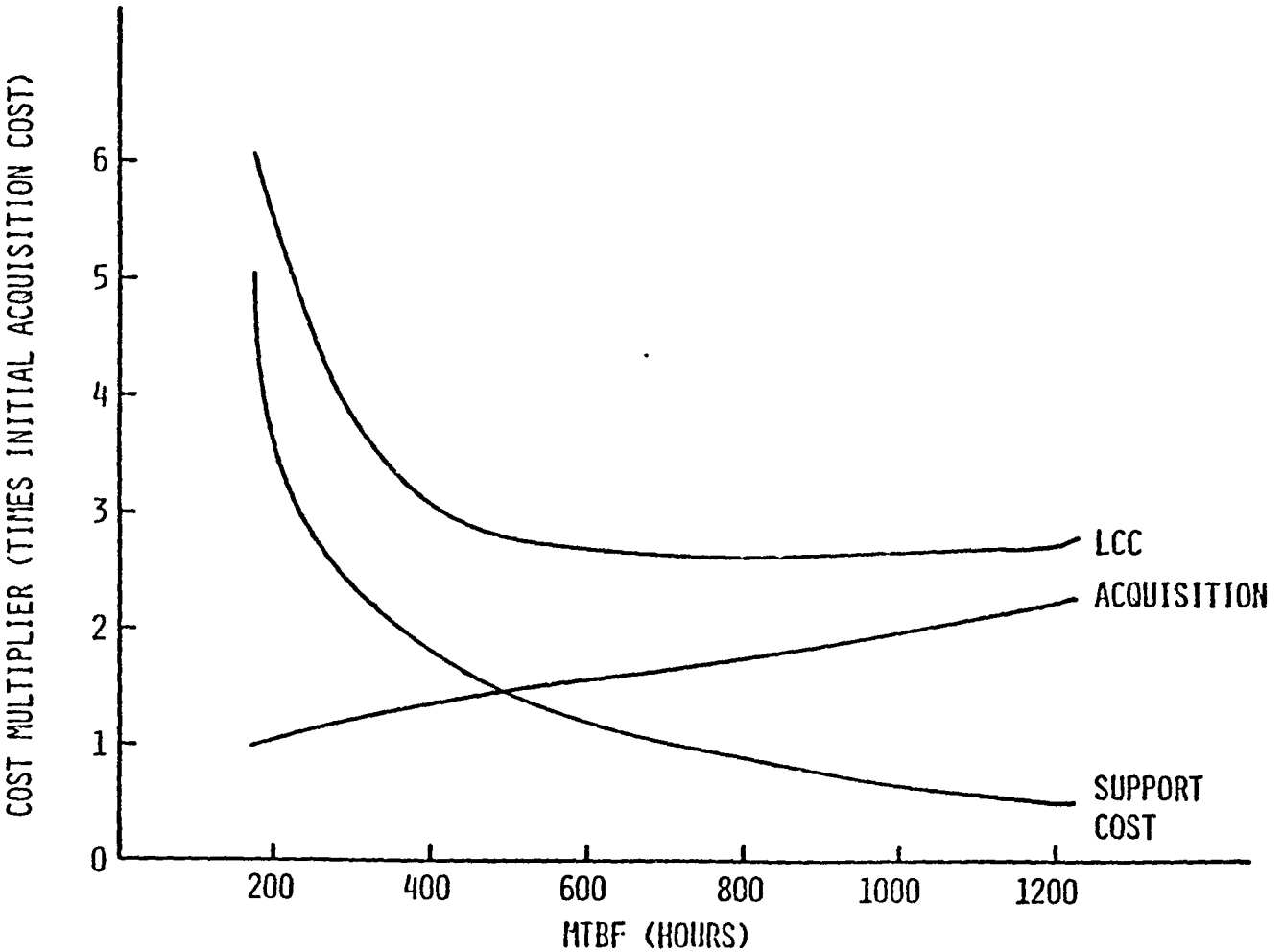


FIGURE 2-1: PREDICTED COST CURVES

2.3 COST (Continued)

impact on LCC. However, if the MIL-grade parts yield an MTBF of 400 hours and the plastic packaged parts have an MTBF of 200 hours, there would then be an order of magnitude difference in LCC.

A cost analysis based upon the specific NASA application should be performed by a Cost Analysis group. This type of analysis will determine the overall life cycle costs and any penalty costs associated with plastic encapsulated devices. As mentioned earlier, field experience has shown (for a benign environment) that the failure rates of equally screened plastic and hermetic devices are very comparable. It is believed that the LCC will not be adversely affected by plastic devices. Detailed failure rates on all types of plastic parts are available from the Parts Engineering organization.

2.4 RISK ASSESSMENT

The decision as to whether or not to use plastic devices will require good communication between the Program Manager and the Design, Parts and Cost Analysis organizations. The basic risks to be considered are:

PROGRAM MANAGER

- Can plastic encapsulated semiconductors meet reliability requirements?
- Are there cost constraints that favor plastic encapsulated devices?
- Are there schedule constraints that favor plastic encapsulated devices?
- Is LCC minimized with plastic encapsulated devices?

DESIGN ENGINEER

- Can performance criteria be satisfied with plastic encapsulated devices?

PARTS ENGINEER

- Are there qualified devices/suppliers?
- Are the devices reliable?
- Are there preferred parts?

If the answer to any or all of these questions is "yes", then there will be a sufficient justification for the use of plastic encapsulated devices.

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SECTION 3.0

SYSTEM DESIGN CONSIDERATIONS

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3.0 SYSTEM DESIGNER CONSIDERATIONS

This section will describe the selection criteria to be used by the designer for determining whether or not to use plastic encapsulated devices in system/subsystem designs. The four main areas of concern for the designer are:

Are the plastic devices on a NASA approved preferred parts list (PPL)?

Performance parameters of specific devices

Availability, particularly of new technology devices

Derating factors such as:

* Thermal - based on system design and packaging
* Voltage - based on devices capabilities and power supply voltages available
* Current - based on power supply capabilities.

Each of these factors will be discussed below.

3.1 UTILIZATION OF PREFERRED DEVICES

All plastic encapsulated devices selected for use in NASA designs should be checked to ensure that they are on the project/NASA Approved Parts List. This parts list will be prepared by the project Parts Engineering organization using parts listed by NASA as acceptable for use in NASA programs subject to lot qualification tests.

3.2 PERFORMANCE PARAMETERS.

The actual system design engineer is usually only concerned about how the individual parts will perform in solving a system design problem. This is not to say that considerations such as cost, realibility and availability should be ignored, but these are often pushed from the forefront by the urgencies of "getting the design released".

It is a common occurrence that circuit designers will use commercial, plastic parts to perform their circuit design breadboarding, and then require very tightly specified parts for their released production design. This desire for tight specification of parameters will present a problem in the use of plastic devices and this problem must be recognized. The problem stems from the fact that the commercial grade plastic encapsulated parts have their parameters specified over only the temperature range of $0^{o}C$ to $70^{o}C$, and the specification is not really a specification at all but merely the manufacturers data sheet. It is true that the manufacturer guarantees that his product will meet the limits of the data sheet, but to collect on the guarantee, the user must perform the required tests and return the failing parts to the manufacturer.

Thus the user of commercial grade parts must be prepared to accept parts that have perhaps wider parameter limits over a narrower temperature range of operation as a consequence of the cost savings afforded by the use of these parts. This applies whether the parts are plastic or commercial hermetic parts. However, in view of the designers proclivity to use the commercial parts in breadboarding, this may not be a great hardship, particularly if the designer can be assured that the parts will be at least 100% tested to the data sheet limits at 25°C and 70° or 100°C as part of the reliability assurance screening process. It is felt that application of imaginative circuit design techniques can overcome any problems that may be caused by use of parts that are tested less rigorously than MIL-specification parts.

The trade off that must be made then by the design engineer, is whether the additional cost of the JAN or equivalent part is justified by the tight specification of its parameters, or whether the looser parameter control of the plastic encapsulated part can be tolerated in the interest of reduced costs. As a general rule, if, in the performance of the worst case analysis, a particular parameter of the plastic devices is not adequately specified, it should not be utilized. If an unspecified (or loosely specified) parameter is not critical to the design, then the plastic device should be used.

3.3 AVAILABILITY

From the design engineers view point, availability means the immediate prospect of obtaining breadboarding and developmental parts, as opposed to the longer range availability of production parts for assembly of deliverable systems. One of the greatest advantages of plastic encapsulated parts is that they are generally available in distributor stock on very short notice, with the result that the designer can proceed expeditiously with his design. In the case of advanced technology parts however, the new devices are generally introduced in hermetic packages, meaning that for these parts the hermetic parts are more available. However, it is these new technology parts that are at the extreme upper end of the cost scale, and switching to the plastic encapsulated version at the earliest opportunity is important from a cost standpoint.

3.3 AVAILABILITY (Continued)

Generally speaking, these new technology parts would not be available in JAN or even military configuration for a long time, by which time the plastic encapsulated parts would be available. Purchase of new technology parts to specification control drawing to achieve the equivalent of a JAN parts results in the most expensive part possible, and thus both cost and availability concerns are answered best by the early choice of plastic encapsulated versions.

3.4 DERATING FACTORS

It has long been a basic tenet of high reliability system design that reliability can be greatly improved by the use of rigorous derating rules on semiconductor operating temperatures, voltages and currents. The Arrhenius activation energy of 1.0 ev is the generally accepted value for all semiconductors with the possible exception of certain failure mechanisms. In fact the manufacturers all dispute the 0.44 ev activation energy called for in MIL-STD-883B, and insist that their data show that 1.0 ev is correct. The impact of a 1.0 ev activation energy on the reliability of semiconductors is shown by acceleration charts (see Table 4-3). These charts indicate that by merely restraining the junction temperature of the semiconductors to 45°C instead of 55°C causes the failure rate to decrease by factor of 3.4, a significant change, and if the junction temperature is reduced still further to 35°C the failure rate would be improved by a total factor of 12.5.

Voltage derating is not normally thought possible with microcircuits, but in the case of CMOS ICs, there is a wide range of operating voltages possible. The experience of several of the users of plastic encapsulated CMOS microcircuits has been that it is desirable to minimize the possible leakage currents in high impedance circuits, thus for CMOS it would be important to use the lowest possible power supply voltage for these devices. The same policy would also seem to apply to NMOS LSI circuits for which there is a choice between those operating at 5 v only as compared to those operating at +12 v, +5 v and -5v. One manufacturer reported that a high voltage screen was useful for the ±5, +12 v memories but not for the +5 v RAMs, indicating that there is a significant difference in the voltage stresses applied to parts at the higher voltage.

3.4 DERATING FACTORS (Continued)

Certain types of advanced NMOS LSI microcircuits employ scaled down geometries to achieve much denser chip layouts. This scaling also affects the oxide thickness, resulting in gate oxides as thin as 400 Angstrons compared to 1100 Angstrons for older ciruits. With a 400 Angstrom gate oxide even a 5 volt device is subjected to extremely high internal voltage stresses and this could pose a reliability problem. Here, the derating process would consist of selection of older unscaled device types that can operate at just 5v instead of $\pm$ 5, 12v, to keep the voltage stresses as low as possible.

While no voltage derating factor can be attached to microcircuits, the message should be that the lowest voltage parts should be chosen when possible. It should be noted that the lowering of supply voltages, particularly on CMOS, may reduce drive capability, noise margin and speed. These factors should be investigated during the design phase.

For discrete semiconductors, the main derating factor identified by the part manufacturers was the junction temperature. The approach used in determining the derating applied to a discrete semiconductor should be that the voltage, current, or both should be derated as much as possible to result in the minimum possible junction temperature. The failure mechanisms of these devices follow the Arrhenius curve in the same manner as microcircuits, and thus an activation energy of 1.0ev can be assumed. Thus, the temperature derating factors of Table 4-3 can be applied to the junction temperature of discrete semiconductors.

SECTION 4.0

PARTS ENGINEERING CONSIDERATIONS

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4.0 PARTS ENGINEER CONSIDERATIONS

4.1 RELIABILITY

The responsibility for assuring the reliability of the plastic encapsulated semiconductors to be used on a NASA project will fall directly upon the parts engineering organization for that project. All possible low cost techniques will have to be employed to control the reliability of the incoming product because of the lack of control over the manufacturer's production processes implied by the use of commercial products as opposed to Mil-qualified products. The techniques to be used in reliability assurance will include:

- Selection of part types that are in high volume production from several manufacturers.
- Qualification tests on sample parts from each of the manufacturers to search for process factors that are out of control.
- Purchase of all parts to a reliability screen that is either the manufacturers high reliability screen (such as SUPR II or PEP) or is a NASA specified screen as defined by a NASA Standard Flow for reliability assurance.
- Application of suitable derating factors to the design guidelines for the use of the parts in the particular NASA system.
- Selection of part types in such a way that known reliability problems are avoided, such as high voltage devices, certain types of CMOS, and devices that operate at high junction temperatures.
- Insistence that the thermal design of the system provide for low thermal resistance for the heat producing semiconductors so as to keep the semiconductor junction temperatures low.
- Plant visits to selected part manufacturers to address particular reliability problems that are uncovered in the qualification and testing process.
- Development of procedures for 100% incoming inspection of all plastic encapsulated semiconductors by all users.
- Publication of parts selection lists design guidelines for the proper selection and application of plastic encapsulated semiconductors by the design engineers.

C - 3

Parts Selection. Perhaps the most important factor to be considered in the selection of plastic encapsulated parts for use in NASA systems is the volume of production for the part types. No parts should be selected that are in limited production or in prototype production. Only parts that are in full production and are widely available in distributor stocks should be selected as candidates for procurement.

The reason for this is that only when a product line is in high volume production will the manufacturer be concerned about the yield to the point where he will institute production controls that will ensure that his product is free from process control problems.

This means that exotic new devices and technologies should be not used in plastic packages, but should be approved for use only as custom specification (Specification Control Drawing) parts, in hermetic packages. The combination of new or exotic technology with the added uncertainties of plastic encapsulation with all its lack of user control over the manufacturers' processes will lead to serious jeopardy of the reliability assurance process. Plastic encapsulated semiconductors can be used reliably, but only if the product is standard, proven, high production product, with production quantities measured in the millions rather than in the thousands.

Qualification Considerations. In addition to the imposition of reliability screening requirements on plastic encapsulated semiconductors, it will be necessary to conduct qualification testing on each lot of parts received for use in deliverable electronics systems. Many of the users of plastic encapsulated devices have in-house programs of device qualification aimed at searching for possible lot oriented problems in the products being purchased.

The qualification approach recommended is one of comparative evaluation of the integrity of the products as received. This means that plastic encapsulated products would be purchased from several sources, subjected to qualification testing and then compared as to their relative performance capabilities in the qualification tests. Any manufacturer's product that is markedly poorer in the response to the tests would be eliminated from the set of parts to be used on the program.

Table 4-1 defines a set of qualification tests that have been suggested as useful by users and manufacturers of plastic encapsulated semiconductors. It is recommended that these tests be built into a NASA standard document for the control of the reliability of plastic encapsulated semiconductors.

The qualification process for a new part type will have to be tailored to each of the technologies considered for use in any NASA program. Different device types require different tests to be applied to uncover any unique process or performance anomolies. There are some basic qualification tests however that can be applied to all products in plastic packages. These are as shown in Table 4-1, consisting of autoclave (pressure pot) tests, temperature-humidity bias (85°C, 85% RH) and some form of high temperature operating life. In addition to these tests, certain device types would require exploratory testing using such stresses as temperature cycling, thermal shock, over-voltage stress testing, and extensive application of three temperature testing (-40°C, 25°C and 125°C or 100°C) of electrical parameters and truth table functionality.

As an example of special tests that might be applied to perform qualification of different devices, it has been found by one user company that linear op-amps can be accelerated to failure by application of a differential input of 24 volts to the input leads. This causes an acceleration factor of 1000, and can be used to compare the relative performance of different manufacturers products under identical test conditions. Such a test set up is shown in Figure 4-1. It is also recommended that delta measurements be made on linear microcircuit parameters. As another example, one manufacturer recommends that in addition to the Table 4-1 qualification tests, an effective qualification test for power transistors would be power cycling tests.

The reason for performing qualification tests is to obtain data to be used in evaluating the integrity of the various manufacturers' products. Most user companies that perform qualification tests compare the results from the different companies and reject the manufacturers whose products seem to deviate from the norm established by the other manufacturers. The decision as to the degree of deficiency must be made by parts engineering organizationson a case by case basis, rather than relying on or even establishing a NASA-qualified list of parts. It can be seen that any overall NASA qualification process would negate the cost advantages afforded by plastic encapsulated parts and thus lead the user to use Mil-qualified hermetic parts instead.

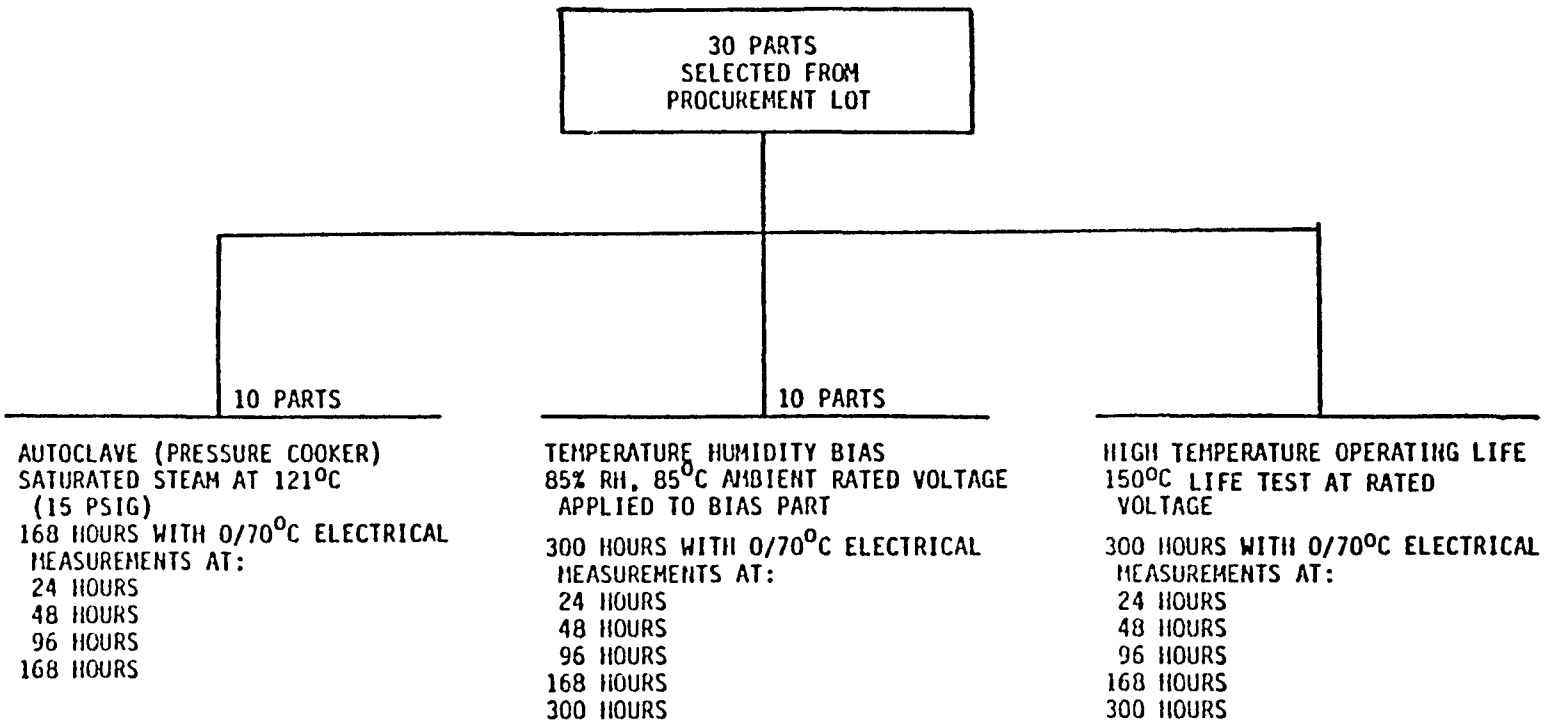

TABLE 4-1

LOT QUALIFICATION TESTS TO BE PERFORMED

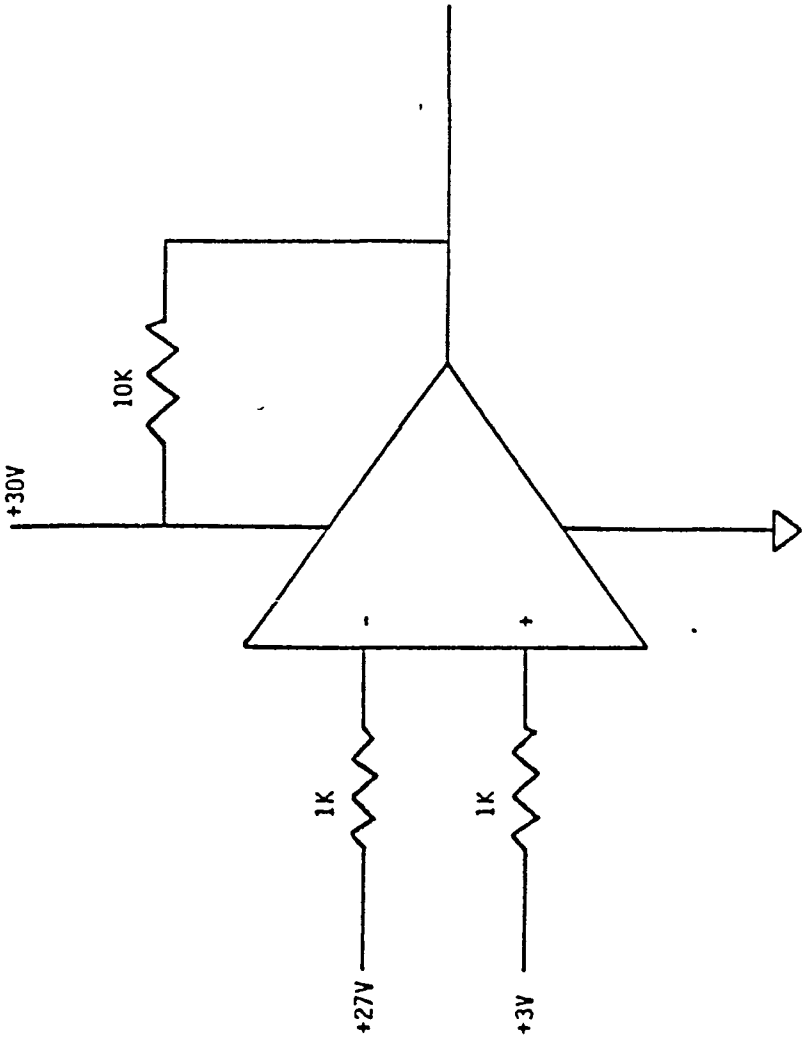

FIGURE 4-1
ACCELERATED STRESS TESTING CIRCUIT FOR LINEAR OP AMPS

Reliability Screening Requirements. Low cost commercial parts of the nature of plastic encapsulated parts have only recently become available with reliability screening performed by the manufacturer. It has been the experience of the users of plastic packaged parts that there is a significant advantage to having some form of reliability screens performed on their parts prior to installation in their systems. And the manufacturers have indicated that there is a significant reliability improvement effected by the use of these screens.

The major decisions facing the parts engineer concerning the use of reliability screens for plastic encapsulated parts revolve around the matter discussed in Table 1-3: none of the manufacturers perform their reliability screening in just the same way, with the result that there is no standardized screen that can be applied to all parts in the same sense as is found with Mil-qualified parts. There are two options available to the parts engineer:

- Call for the parts to be screened to a NASA Standard Flow which is to be defined and negotiated by further work with the manufacturers, but which would resemble Table 4-2.
- Call for the manufacturers to perform parts screening to their own in-house programs where these programs are available for the part types of interest (see Tables 1-3, 1-4). Of the various options available for manufacturers' in-house screening, the following minimum screens for microcircuits should be covered:
  - * Temperature cycling
  - * Pre-burn-in electrical measurement or functional test
  - * Burn-in for the equivalent of 168 hours at 125°C
  - * Post-burn-in electrical measurement

Note that the proposed NASA standard flow for microcircuits can easily include a requirement for burn-in, since the manufacturers already have the capability to perform this screen. But for discrete semiconductors such as transistors and diodes, the manufacturers generally do not have any burn-in facilities and would not agree to performing any type of burn-in. It is recommended that alternate tests should be employed to assure the integrity of the discrete semiconductors parts. These tests are as shown in Table 4-2 for transistors. In the event that burn-in of discrete semiconductors is really felt to be an important ingredient

TEMPERATURE CYCLING	30 CYCLES: $0^{o}C$ to $100^{o}C$, GAS TO GAS
100% FUNCTIONAL TEST	$70^{o}C$, $25^{o}C$
100% DC PARAMETERS	$70^{o}C$, $25^{o}C$
BURN-IN	168 HOURS AT $125^{o}C$ (OR EQUIVALENT USING 1.0ev ACTIVATION ENERGY) θ $<150^{o}C$
100% FUNCTIONAL TEST PERFORMED TWICE (TWO PASSES)	$70^{o}C$ $25^{o}C$
100% DC PARAMETERS TEST PERFORMED TWICE (TWO PASSES)	$70^{o}C$ $25^{o}C$

TABLE 4-2A

PROPOSED NASA STANDARD FLOW FOR
RELIABILITY SCREENING OF PLASTIC ENCAPSULATED MICROCIRCUITS

SCREEN	POWER TRANSISTORS	SMALL SIGNAL TRANSISTORS	ZENER DIODES	RECTIFIERS
TEMPERATURE CYCLING	30 CYCLES 0 TO 100°C (GAS TO GAS)			
100% FUNCTIONAL AND PARAMETRIC TESTS	100° (RELAXED LIMITS) AND 25°C			
100% SPECIAL OVERSTRESS SCREEN	SAFE OPERATING AREA (SOA) VBEF AT RATED I_C 300μsec	VBEF AT RATED I_C: 300μsec	SURGE TEST: 100ms PULSE, 10X RATED POWER OF DIODE	HTRB 48 HR @ 125°C
100% PARAMETRIC TESTS (TWO PASSES AT EACH TEMPERATURE)	70°C AND 25°C			

TABLE 4-28

PROPOSED NASA STANDARD FLOW FOR RELIABILITY SCREENING OF PLASTIC ENCAPSULATED DISCRETE SEMICONDUCTORS

of a particular NASA program, the decision should then be made to use JANTX parts instead, since these parts do receive burn-in and the cost differential is minimal.

In the course of the discussions held with both users of plastic packaged parts and the manufacturers of the parts, a number of special screens were identified that would be desirable but which would entail a significant cost adder to implement.

- Overvoltage stress tests. Effective for some parts but expensive to implement because it requires changing of automatic tester test tapes.
- Delta measurements on certain linear microcircuit parameters before and after burn-in.
- Temperature cycling over a wider temperature range than normally performed.

The trouble with special screens above and beyond the standard reliability screens performed in-house by the manufacturers is that they upset the normal flow of parts through the extremely high volume production and delivery cycle. Anything that forces the manufacturer to perform unusual handling or testing that differs from his normal flow generally causes significant cost increases. Most manufacturers perform their reliability screening at their off-shore facilities, and the paper work and special handling required to achieve custom screening present formidable logistics problems.

For this reason it would be imperative that NASA develop and negotiate an agreeable set of reliability screens (a NASA Standard Flow) for plastic encapsulated parts that all manufacturers could agree to, if it should be necessary to try to screen all parts from all manufacturers in the same manner. Table 4-2 lists the screens for individual part types.

Derating. Each NASA system will have different operational characteristics that will require differing parts application requirements. It will be the function of the parts engineer to interpret these program-unique characteristics and define the derating factors necessary for each of the parts types selected for use on the program. Derating will have to take into account the standard

factors of voltage stress, current stress and thermal stress associated with any high performance design, but in addition, there must be derating factors applied to the plastic encapsulated parts used on the program.

The primary derating factor of concern for plastic packaged parts is the voltage stress applied to the parts. Data from the industrial users of plastic encapsulated parts indicate that the failure rates for high voltage parts is generally higher than for the low voltage parts, particularly for transistors. For CMOS microcircuits, it would be recommended that the lowest possible supply voltage be used in any design, since there seems to be a correlation between Vcc voltage and failure rate, both from the users standpoint and from the manufacturers qualification test data. The manufacturers of transistors and rectifier diodes also recommended that the voltage be derated on these devices by selection of higher rated parts for particular applications. While the same precautions probably should be applied to hermetic parts as well, there seems to be a feeling in the industry that the migration of ionic contaminants is accelerated in plastic encapsulated semiconductors by the application of high voltages, and thus it seems prudent to derate the applied voltages as much as possible.

The reliability of semiconductors can also be improved by lowering the junction temperature of the devices. Table 4-3 shows the acceleration factors for failure rates at different operating temperatures. In general, the operating junction temperature should be minimized to maximize reliability.

Parts Selection. The primary duty of the parts engineer in the selection of plastic encapsulated parts for NASA applications is the identification of those part types from manufacturers that pose reliability problems stemming from out-of-control processes. It will be the function of the parts engineer, based on the results of the qualification test data and other data sources, to tell the design engineers about the parts that must not be used on the specific program.

Since there will be a NASA Parts Selection List (PSL) or Preferred Parts List (PPL) for plastic encapsulated semiconductors, the parts engineers must interpret the particular system design requirements in terms of the device types available and thereby create a program approved parts list. This list is necessary for the designer to list the parts he needs on his assembly drawing parts lists. The particular manufacturers' part numbers that are found to be undesirable for use in a program must be identified to materiel and to the assembly shop, so that precautionary measures can be taken to make sure that the suspect parts do not get installed into deliverable systems.

T_2 °C ↓	T_1 (°C) → 25	35	45	55	65	75	85	95	105	115	125
25	1										
35	3.6	1									
45	14	3.3	1								
55	45	11.3	3.1	1							
65	143	36	10	2.9	1						
75	423	105	29	8.4	2.7	1					
85	1180	293	80	24	7.4	2.5	1				
95	3090	771	210	62	19	6.6	2.4	1			
105	7730	1480	520	120	49	16.5	6.0	2.3	1		
115	18,500	4600	1250	370	117	39.4	14.2	5.4	2.2	1	
125	42,100	10,500	2860	840	266	90.1	32.3	12.3	4.9	2.1	1
135	92,300	23,000	6260	1850	584	197	71	27	10.8	4.5	2.0
145	195,000	48,600	13,210	3890	1230	417	150	57	23	9.6	4.2
155	397,000	98,600	27,100	7940	2520	850	306	116	46.5	19.5	8.5

Accel. Factor: $\frac{FR(T2)}{FR(T1)} = Exp\left(\frac{1.0}{8.63 \times 10^{-5}}\left[\frac{1}{273+T1} - \frac{1}{273+T2}\right]\right)$

T = Temperature, °C

$FR(T_2)$ = Failure rate at T_2

$FR(T_1)$ = Failure rate at T_1

(Based on Ea. = 1.0 ev)

TABLE 4-3

ACCELERATION FACTORS FOR FAILURE RATES AT DIFFERENT OPERATING TEMPERATURE

Another area of parts selection that must be addressed by the parts engineer is the choice between specific technologies in terms of acceptable reliability or failure rates. Table 4-4 lists microcircuit failure rates and Table 4-5 lists transistor failure rates for a wide variety of parts as reported by various industrial users of plastic encapsulated semiconductors. Based on the conservative factor of 5:1 for the improvement in reliability afforded by burn-in screening, burned-in commercial plastic encapsulated parts could be expected to have lower failure rates than unburned-in parts as reported by the users, and this is shown by the second column of data. Table 4-4 also lists (third column) the failure rates that the manufacturers claim for their parts in the non-burned-in configuration. The fourth column of data presents the failure rates reported by RAC for hermetic microcircuits in certain selected categories; these parts were screened to the requirements of MIL-STD-883 Class B, by the manufacturers, but were not JAN Class B microcircuits.

Thermal Design. It is not enough for the parts engineer to insist on thermal derating of the parts to be used on a program. He also has the responsibility to insist that the thermal design of the system will provide the low thermal resistance paths necessary to keep the semiconductor junction temperatures within the limits called for in the thermal derating plan. This means that the parts engineer must participate in the design reviews for the thermal design to argue for the reliability needs of the electronic parts. The particular problem faced by the use of plastic encapsulated parts is that these parts cannot stand extended exposure to internal temperatures greater than $150^{o}C$ because of the degradation of the plastic material that results above this temperature.

Plant Visits. Suppliers of plastic encapsulated parts should be visited by the parts engineering organization for each project to negotiate and solicit their active cooperation in meeting the reliability objectives of the particular NASA program. This will be particularly true when the NASA Standard Flow is developed for screening parts in a manner different than the manufacturers' existing reliability screening process. It is also improtant that the manufacturers be made aware of problems that are uncovered by the qualification testing done on incoming part lots. These can often be best communicated by

TECHNOLOGY	YEAR	ACTUAL FIELD FAILURE RATE RANGE		EXPECTED FAILURE RATE RANGE IF BURNED IN		MANUFACTURERS PREDICTED 55°C FAILURE RATE, NO BURN IN		JAN LEVEL B OR SCREENED TO JAN LEVEL B (BURNED IN)(b)	
		1/ MIN	1/ MAX	1/ MIN	1/ MAX	1/ MIN	1/ MAX	1/ MIN	1/ MAX
SSI BIPOLAR MICROCIRCUIT									
TTL	1978	.0045	.03	.0009	.006	.00068	.0041	.0022	.11
LSTTL	1978	.002	.005	.0004	.001	.0005	.0012		
STTL	1977,78	.018	.033	.0036	.033				
ECL	1978	.02	.04(b)	.004	.008(b)				
LINEAR AMP	1978	.025	.09	.005	.0018	.0039	.0125		
FIXED VOLTAGE REGULATOR (a)	1978	.045	.075	.009	.015	.01			
VARIABLE VOLTAGE REGULATOR (a)	1978	.1	.15	.02	.03				
MSI BIPOLAR MICROCIRCUITS									
TTL	1978	.013	.024	.0026	.0048	.0041		.0068	.15
LSTTL	1978	.004	.042	.001	.008				
STTL	1977	.007	.45	.0014	.09	.0041			
ECL (b)	1977,78	.036	.044	.0072	.0088				
LSI BIPOLAR MICROCIRCUITS									
STTL & RAM	1974	.03	.07	.006	.014	.0088	.138	.016	.71
SSI CMOS LOGIC MICROCIRCUITS									
PLASTIC	1977,78	.01	.25	.002	.05	.001	.005		
HERMETIC (b)	1977,78	.03	.05	.006	.01	.0016			
LSI NMOS MICROCIRCUITS									
MICROPROCESSOR	1977,78	.05	.17	.01	.034	.0065	.05		
MEMORY	1977,78	.045	.07	.009	.014	.0051	.025	.087	.12

1/ %/1000 hours

TABLE 4-4

FIELD USAGE MICROCIRCUIT FAILURE RATES IN PERCENT PER 1000 HOURS

(a) HERMETIC AND PLASTIC BOTH INCLUDED
(b) HERMETIC

TRANSISTOR TYPE		YEAR	ACTUAL FIELD FAILURE OR REMOVAL RATES MIN	MAX
BIPOLAR SMALL SIGNAL				
NPN	PLASTIC	1977,78	.0053	.08
	HERMETIC	1977,78	.02	.1
PNP	PLASTIC	1978	.017	
	HERMETIC	1978		.025
BIPOLAR POWER				
NPN	PLASTIC	1978	.05	.13
	HERMETIC	1977,78	.068	.098
PNP	PLASTIC	1977,78	.036	
	HERMETIC	1977,78		.06
JFET SMALL SIGNAL				
	PLASTIC	1978	.045	.075
	HERMETIC	1978	.006	.04

TABLE 4-5

FIELD USAGE TRANSISTOR FIALURE RATES IN PERCENT PER 1000 HOURS

means of plant visits. The main point in the conduct of plant visits is that the use of plastic encapsulated semiconductors requires a close working relationship between the user and the manufacturer, if the acceptable reliability is to be maintained. This relationship cannot be maintained by purchase orders, but requires face-to-face contact.

Incoming Inspection. In addition to the 100% electrical testing done by the manufacturer, (and even redundant 100% testing as suggested by the NASA Standard Flow) each user of plastic encapsulated semiconductors must be prepared to perform 100% incoming receiving inspection. This should consist of 100% electrical measurement of the electrical parameters and functionality at least at 25°C and at other temperatures if possible. The parts engineering organization will be responsible for defining the electrical test requirements to the quality assurance organization that will perform the receiving inspection.

Parts Selection Lists and Design Guidelines. The parts engineering organization will be responsible for preparation of the appropriate documentation for communication of the plastic parts technical information to the design engineers and other management personnel affected by the decision to use plastic encapsulated semiconductors. The NASA part Selection Lists will have to be interpreted and translated into the needs of the particular project with exclusions and additions as necessary to meet project performance and reliability needs. In addition, NASA design guidelines will have to be related to the particular system under design to effect a maximum match between the capabilities of plastic packaged parts and the requirements of the system.

4.2 AVAILABILITY

One of the reasons advanced for the use of plastic encapsulated semiconductors is that because of the immense quantities of the parts produced there should be much better availability of these parts than for Mil-qualified parts. This situation is not always the case, however, and is a changing picture depending on the demand for each individual part type. A figure such as Figure 1-2 should be constructed by cooperative efforts between the parts engineers and the materiel organization so that parts which exhibit long lead times can be avoided. As a general rule, selection of parts that have several suppliers will result in improved availability of the parts, even though the demand might be quite

high. In view of the reluctance of some manufacturers to agree to perform special screens, even to a NASA Standard Flow, it might be expected that the imposition of any special screens for reliability improvement would result in aggravation of the availability problem. However it will be found that while one manufacturer might be reluctant to comply, the next one will be very cooperative and agreeable, with the result that availability might not be difficult at all. The significant factor to be considered is that every part number in a parts list must have a separate determination of its availability made on a continuing basis (say month by month) to ensure that the right types of parts are selected for production assembly. This will permit the tradeoff to be made between delivery schedules, cost and reliability.

One other factor to be considered in the analysis of the availability question is choice or avoidance of advanced technology parts. Designers have a way of wanting to use the most advanced parts possible, whether they are available or not. If advanced technology parts such as certaun large, fast memories are selected and the manufacturer is only shipping parts on allocation (only a certain percentage of each order will be filled each month), then severe program schedule delays will result. Generally speaking, the advanced part types are introduced in hermetic packages rather than plastic packages, with the result that if the program is counting on low cost plastic parts and only hermetic parts are available, the schedule picture could be dangerous. The solution would be to encourage designers to emphasize more mature technology parts in their designs, particularly when plastic encapsulated parts are to be used.

4.3 COST

The question of cost advantages for plastic parts has been covered briefly in Section 1, where an example was given for the cost adders involved with plastic encapsulated semiconductors purchased to several reliability screening options. Detailed cost data are not currently available for all of the manufacturers of plastic devices. The data are going to have to be obtained by formal requests for budgetary estimates for performing the NASA Standard Flow on each of various part types under consideration. When these data become available, they will be added to this document for additional guidance in the development of a rationale for the use of plastic encapsulated semiconductors.

One of the things that must be recognized in the comparison of costs between plastic packaged parts and hermetic parts (particularly JAN products) is the cost of parts engineering and parts qualification that must be added to the plastic parts. Since the JAN parts are already qualified, the parts engineering costs are somewhat reduced. However, for the commercial parts, where is a significant cost for negotiation of purchase agreements, performing qualification tests, monitoring of the manufacturers, follow up on parts that fail qualification, and maintenance of standard parts lists that cover all of the approved manufacturers' part numbers. These costs must be added onto the purchase costs at a rate determined by dividing the total costs per part number by the total quantity of the part to be purchased for the program. If, for example, it takes three man months (480 hours) to perform all of the parts engineering and qualification testing on a single part number from one manufacturer, the cost would be approximately 480 hours x $40 per hour, or $19,200 for the lot of parts. If the purchase quantity is only 1000 parts, the cost adder would be $19.20 per part to be added onto the approximately $.50 per part purchase cost.

If however, the qualification tests could be extended to an entire family of 30 part types, resulting in the $19,200 parts engineering cost being spread of 30,000 parts instead, then the parts engineering cost adder would only by $.64 per part to be added to the $.50 purchase cost. The specific cost trade offs would have to be computed for each project and for each set of parts.

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APPENDIX

FIELD DATA

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TABLE 1: . FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
209	73	J	DIODE BRIDGE ASSY	-	16	5	P	1.1 E8	.00089	0
208	73	J	DIODE LED	-	16	5	P	9.1 E8	.0010	8
038	77	B	DIODE LED	-	17	7	P	2.7 E6	.012	
204	73	J	DIODE PWR	-	16	5	P	1.9 E9	.0034	62
206	73	J	DIODE REF	-	16	5	P	5.6 E8	.062	337
197	76	H	DIODE SS	-	17	5	P	1.7 E10	.001	
037	77	B	DIODE SS	-	17	7	P	2.8 E9	.0074	
203	77	H	DIODE SS	-	17	5	P	8.7 E8	.0016	28
205	73	J	DIODE SWITCHING	-	16	5	P	2.7 E11	.00058	1571
207	73	J	DIODE ZENER	-	16	5	P	4.0 E8	.0018	6
122	78	F	LSI BIPOLAR PROM	-	16	5	P	8.4 E6	.011	0
281	72	SA	LSI BIPOLAR RAM	-	16	6	P	4.1 E6	.128	
259	76	RAC	LSI CMOS COUNTER	4020	13	5	P	4.5 E6	.021	0
252	76	RAC	LSI ECL PROM	1307	13	5	P	8.8 E6	.023	1
007	74	A	LSI LINEAR	-	16	5	P	1.6 E6	.058	0
015	74	A	LSI LINEAR	-	16	5	H	2.4 E5	-	0
024	74	A	LSI LINEAR	-	16	5	P	7.4 E6	.012	0
032	74	A	LSI LINEAR	-	16	5	H	1.1 E6	.082	0
017	74	A	LSI NMOS	-	16	5	H	9.3 E5	-	0
034	74	A	LSI NMOS	-	16	5	H	4.2 E6	.022	0
168	76	G	LSI NMOS MPROC	UP6800	16	5	P	1.1 E7	.05	
257	76	RAC	LSI NMOS MPROC	3850	12	9	P	4.3 E7	1.1	462
169	77	G	LSI NMOS MPROC	UP6800	11	5	P	1.4 E7	.157	
258	77	RAC	LSI NMOS MPROC	Z80	13	5	P	4.7 E6	.16	6
253	76	RAC	LSI NMOS RAM	2102	13	5	P	1.2 E6	.076	0
254	77	RAC	LSI NMOS RAM	4096	13	5	P	6.4 E6	.049	2
264	77	RAC	LSI NMOS RAM	4096	13	5	H	3.1 E6	.17	4
121	78	F	LSI NMOS RAM	-	16	5	P	3.3 E6	.026	0
165	76	G	LSI NMOS 1KRAM	2102	16	5	P	5.7 E7	.06	
166	77	G	LSI NMOS 1KRAM	2102	16	5	P	1.2 E8	.07	
167	78	G	LSI NMOS 1KRAM	2102	16	5	P	1.0 E8	.055	
219	73	J	LSI PMOS	1404	16	5	H	2.3 E9	.011	236
226	75	J	LSI PMOS	1404	12	5	H	4.2 E6	.022	0
263	75	RAC	LSI PMOS	-	13	6	H	1.8 E7	.13	22
192	76	H	LSI PMOS	-	17	5	P	3.6 E8	.045	
261	76	RAC	LSI PMOS	5009	13	5	H	1.2 E7	.15	16
262	76	RAC	LSI PMOS	1013	13	5	H	1.0 E7	.11	9
039	77	B	LSI PMOS	-	17	8	P	0.5 E6	.25	
199	77	H	LSI PMOS	-	17	5	P	5.1 E7	.005	31
230	77	RAC	LSI PMOS	-	13	7	P	2.4 E8	.029	67
040	78	B	LSI PMOS	-	17	8	P	0.5 E6	.016	
276	72	SA	LSI PMOS CHAR GEN	-	16	6	P	8.22E6	.029	
280	72	SA	LSI PMOS RAM	-	16	6	P	5.0 E8	.019	
277	72	SA	LSI PMOS ROM	-	16	6	P	5 E7	.0078	
279	72	SA	LSI PMOS S/R	-	16	6	P	1.6 E7	.041	
255	76	RAC	LSI PMOS S/R	5007	13	5	P	2.5 E7	.12	28
110	73	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
113	73	D	LSI RAM	MODULE	12	4	C	8.7 E6	.31	25
111	74	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
114	74	D	LSI RAM	MODULE	12	4	C	8.8 E6	.20	17
112	75	D	LSI RAM	MODULE	12	4	C	9.2 E5	.22	1

TABLE 1: FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F/
008	74	A	LSI STTL	-	16	5	P	1.6 E6	.058	0
016	74	A	LSI STTL	-	16	5	M	3.2 E6	.025	0
025	74	A	LSI STTL	-	16	5	P	9.6 E6	.044	3
033	74	A	LSI STTL	-	16	5	M	1.4 E6	.063	0
132	76	G	MSI ECL	10102	16	5	M	2.9 E7	.10	
133	77	G	MSI ECL	10102	16	5	M	7.2 E7	.033	
134	78	G	MSI ECL	10102	16	5	M	7.8 E7	.044	
005	74	A	MSI HTTL	-	16	5	P	5.1 E6	.018	0
014	74	A	MSI HTTL	-	16	5	M	8.0 E5	.25	1
023	74	A	MSI HTTL	-	16	5	P	2.3 E7	.027	5
031	74	A	MSI HTTL	-	11	5	M	3.5 E6	.026	0
235	77	RAC	MSI LSTTL	-	12,13	4	P	2.3 E7	.024	0
251	77	RAC	MSI LSTTL	25LS15	12	5	P	2.6 E6	.036	0
173	76	G	MSI LSTTL FF	74LS74	16	5	P	3.6 E7	.013	
174	77	G	MSI LSTTL FF	74LS74	16	5	P	8 E7	.008	
175	78	G	MSI LSTTL FF	74LS74	16	5	P	2.0 E8	.008	
217	73	J	MSI LTTL	-	16	5	P	3.7 E9	.066	242
256	71	RAC	MSI PMOS	-	13	9	P	2.6 E9	.052	1321
005	74	A	MSI STTL	-	16	5	P	2.2 E7	.039	7
013	74	A	MSI STTL	-	16	5	M	3.3 E6	.028	0
022	74	A	MSI STTL	-	16	5	P	1.1 E8	.0076	7
030	74	A	MSI STTL	-	16	5	M	1.7 E7	.0055	0
250	76	RAC	MSI STTL	-	13	5	P	5.2 E7	.036	17
260	76	RAC	MSI STTL	3207A	13	5	M	3.5 E6	.026	0
234	77	RAC	MSI STTL	-	13	4	P	1.1 E7	.019	1
244	77	RAC	MSI STTL	-	5	7,10	M	2.4 E6	.038	0
185	76	G	MSI STTL FF	74S74	16	5	P	5.4 E6	.04	
186	77	G	MSI STTL FF	74S74	16	5	P	1.5 E7	.007	
187	78	G	MSI STTL FF	74S74	16	5	P	2.2 E7	.0142	
218	73	J	MSI TTL	-	16	5	P	3.1 E9	.012	351
004	74	A	MSI TTL	-	16	5	P	9.6 E7	.025	22
012	74	A	MSI TTL	-	16	5	M	1.5 E7	.014	1
021	74	A	MSI TTL	-	16	5	P	7.3 E8	.0076	53
029	74	A	MSI TTL	-	16	5	M	1.1 E8	.0006	0
222	75	J	MSI TTL	-	12	5	P	5.78 E6	.016	0
236	77	RAC	MSI TTL	-	13	4	P	3.2 E6	.13	3
237	77	RAC	MSI TTL	-	12	4	P	4.9 E6	.019	0
245	77	RAC	MSI TTL	-	5	3,6	M	4.8 E7	.0019	0
246	77	RAC	MSI TTL	-	6	3	M	1.3 E6	.16	1
247	77	RAC	MSI TTL	-	4	6,10	M	8.3 E7	.0011	0
248	77	RAC	MSI TTL	-	10	2,3	M	3.4 E7	.025	7
249	77	RAC	MSI TTL	-	13	7	M	1.7 E6	.054	0
275	72	SA	MSI TTL FF	-	16	6	P	5.6 E8	.022	
179	76	G	MSI TTL FF	7474	16	5	P	2.4 E8	.024	
180	77	G	MSI TTL FF	7474	16	5	P	2.3 E8	.021	
119	78	F	MSI TTL FF	-	16	5	P	6.6 E6	.014	0
181	78	G	MSI TTL FF	7474	16	5	P	3.2 E8	.0235	
274	72	SA	MSI TTL GATE	-	16	6	P	1.7 E8	.023	
118	78	F	MSI TTL GATE	-	16	5	P	7.7 E6	.012	0
214	73	J	PHOTO ISOLATOR	-	16	5	P	2.0 E9	.630	61
144	76	G	SCR	C10682	16	5	P	1.6 E7	.092	

TABLE 1: FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAI
145	77	G	SCR	C106B2	16	5	P	1.8 EE	.116	
146	78	G	SCR	C106B2	16	5	P	1.9 E7	.09	
191	76	H	SSI CMOS	-	17	5	P	2.5 E9	.004	
198	77	H	SSI CMOS	-	17	5	P	5.1 E7	.0026	4
229	77	K	SSI CMOS	-	11	5	P	4.9 E7	.017	7
115	78	F	SSI CMOS GATE	MEM4900P	12	5	P	8.4 E5	.24	1
098	76	C	SSI ECL	-	13	5	H	1.7 E7	.066	11
101	76	C	SSI ECL	-	13	5	P	9.3 E7	.041	38
099	77	C	SSI ECL	-	13	5	H	6.8 E7	.038	26
102	77	C	SSI ECL	-	13	5	P	2.5 E8	.029	70
100	78	C	SSI ECL	-	13	5	H	1.0 E8	.035	35
103	78	C	SSI ECL	-	13	5	P	2.5 E8	.021	51
129	76	G	SSI ECL GATE	10102	16	5	H	3.9 E7	.039	
130	77	G	SSI ECL GATE	10102	16	5	H	6 E7	.031	
131	78	G	SSI ECL GATE	10102	16	5	H	7.5 E7	.039	
003	74	A	SSI HTTL	-	16	5	P	1.3 E8	.013	15
011	74	A	SSI HTTL	-	16	5	H	2.0 E7	.0045	0
020	74	A	SSI HTTL	-	16	5	P	7 E8	.003	19
028	74	A	SSI HTTL	-	16	5	H	1.1 E8	.0008	0
270	72	SA	SSI LIN	-	16	6	P	1.0 E7	.028	
271	77	K	SSI LIN	CUSTOM	12	8	P	5.2 E7	.0079	
043	77	B	SSI LN AM PWR	-	17	7	P	4 E7	.05	
080	76	C	SSI LN OP AMP	-	13	5	H	7.7 E8	.051	39.
083	76	C	SSI LN OP AMP	-	13	5	P	8.7 E7	.008	59
193	76	H	SSI LN OP AMP	741	17	5	P	3.6 E9	.001	
194	76	H	SSI LN OP AMP	1458	17	5	P	4.0 E9	.002	
041	77	B	SSI LN OP AMP	-	17	7	P	8.1 E9	.05	
081	77	C	SSI LN OP AMP	-	13	5	H	1.5 E9	.050	72.
084	77	C	SSI LN OP AMP	-	13	5	P	1.8 E8	.026	13
163	77	G	SSI LN OP AMP	LM741	16	5	P	3 E8	.067	
200	77	H	SSI LN OP AMP	1458	17	5	P	2.0 E8	.010	4
082	78	C	SSI LN OP AMP	-	13	5	H	7.7 E8	.039	30
085	78	C	SSI LN OP AMP	-	13	5	P	1.1 E8	.022	24
120	76	F	SSI LN OP AMP	-	16	5	P	3.4 E6	.027	0
164	78	G	SSI LN OP AMP	LM741	16	5	P	3.9 E8	.087	
162	76	G	SSI LN OP AMP	LM741	16	5	P	3 E8	.101	
220	73	J	SSI LN VLT REG	-	16	5	P	2.8 E9	.011	30
225	75	J	SSI LN VLT REG	-	12	5	P	4.0 E6	.023	0
227	75	J	SSI LN VLT REG	-	12	5	H	4.0 E6	.023	0
086	76	C	SSI LN VLT RG FIX	-	13	5	H	3.3 E7	.090	30
088	76	C	SSI LN VLT RG FIX	-	13	5	H	5.0 E7	.070	35
089	76	C	SSI LN VLT RG FIX	-	13	5	P	4.1 E7	.092	38
153	76	G	SSI LN VLT RG FIX	-	16	5	P	1.47 E7	.127	
042	77	B	SSI LN VLT RG FIX	-	17	7	P	2.2 E9	.11	
087	77	C	SSI LN VLT RG FIX	-	13	5	H	4.5 E7	.062	50
090	77	C	SSI LN VLT RG FIX	-	13	5	P	1.1 E8	.103	11
154	77	G	SSI LN VLT RG FIX	-	16	5	P	1.7 E7	.12	
091	78	C	SSI LN VLT RG FIX	-	13	5	P	7.4 E7	.045	33
155	78	G	SSI LN VLT RG FIX	-	16	5	P	2.7 E7	.073	
092	76	C	SSI LN VLT RG VAR	-	13	5	H	1.2 E6	.122	14
095	76	C	SSI LN VLT RG VAR	-	13	5	P	6.3 E6	.320	20

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TABLE 1: FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F. J
156	76	G	SSI LN VLT RG VAR	-	16	5	H	4.8 E7	.175	
093	77	C	SSI LN VLT RG VAR	-	13	5	H	2.6 E8	.112	296
096	77	C	SSI LN VLT RG VAR	-	13	5	P	1.5 E7	.298	44
157	77	G	SSI LN VLT RG VAR	-	16	5	H	4.5 E7	.17	
094	78	C	SSI LN VLT RG VAR	-	13	5	H	1.2 E8	.100	118
097	78	C	SSI LN VLT RG VAR	-	13	5	P	1.1 E7	.140	16
158	78	G	SSI LN VLT RG VAR		16	5	H	5.9 E7	.124	
224	75	J	SSI LSTTL	-	12	5	P	1.80 E7	.0051	0
232	77	RAC	SSI LSTTL	-	12,13	4	P	1.3 E6	.07	0
170	76	G	SSI LSTTL GATE	74LS00	16	5	P	3.8 E7	.01	
171	77	G	SSI LSTTL GATE	74LS00	16	5	P	1.0 E8	.005	
172	78	G	SSI LSTTL GATE	74LS00	16	5	P	2 E8	.002	
215	73	J	SSI LTTL	-	16	5	P	1.4 E10	.0047	656
002	74	A	SSI STTL	-	16	5	P	1.9 E7	.0049	0
010	74	A	SSI STTL	-	16	5	H	3.6 E6	.026	0
019	74	A	SSI STTL	-	16	5	P	1.1 E8	.0029	2
027	74	A	SSI STTL	-	16	5	H	1.6 E7	.006	0
223	75	J	SSI STTL	-	12	5	P	1.77 E6	.052	0
231	77	RAC	SSI STTL	-	12,13	4	P	6.8 E6	.014	0
238	77	RAC	SSI STTL	-	5	6,10	H	4.4 E6	.021	0
182	76	G	SSI STTL GATE	74S00	16	5	P	3.6 E7	.017	
183	77	G	SSI STTL GATE	74S00	16	5	P	4.5 E7	.018	
184	78	G	SSI STTL GATE	74S00	16	5	P	8.1 E7	.02	
265	72	SBM	SSI TTL	-	12	4	H	1.5 E7	.028	3
266	72	SBM	SSI TTL	-	12	4	H	9.9 E6	.054	4
267	72	SBM	SSI TTL	-	17	4	H	4.7 E6	.043	1
268	72	SBM	SSI TTL	-	12	4	P	3.3 E6	.028	0
269	72	SBM	SSI TTL	-	12	4	P	8.4 E6	.024	1
270	72	SBM	SSI TTL	-	17	4	P	1.5 E7	.022	2
216	73	J	SSI TTL	-	16	5	P	9.1 E9	.0090	807
001	74	A	SSI TTL	-	16	5	P	1.5 E7	.042	5
009	74	A	SSI TTL	-	16	5	H	2.3 E6	.04	0
018	74	A	SSI TTL	-	16	5	P	1.3 E8	.005	5
026	74	A	SSI TTL	-	16	5	H	1.9 E7	.005	0
221	75	J	SSI TTL	-	12	5	P	1.02 E6	.090	0
228	77	K	SSI TTL	-	11	5	P	4.9 E7	.015	6
233	77	RAC	SSI TTL	-	12,13	4	P	5.5 E6	.017	0
239	77	RAC	SSI TTL	-	4	6,10	H	7.4 E7	.0027	1
240	77	RAC	SSI TTL	-	5	3	H	1.7 E7	.012	1
241	77	RAC	SSI TTL	-	6	3	H	5.8 E6	.11	5
242	77	RAC	SSI TTL	-	10	2	H	1.7 E7	.025	3
243	77	RAC	SSI TTL	-	13	7	H	2.6 E6	.036	0
273	72	SA	SSI TTL FF	-	16	6	P	3.2 E8	.022	
117	78	F	SSI TTL FF	-	16	5	P	5.5 E6	.017	0
272	72	SA	SSI TTL GATE	-	16	6	P	1.9 E9	.012	
176	76	G	SSI TTL GATE	7400	16	5	P	3.4 E8	.021	
177	77	G	SSI TTL GATE	7400	16	5	P	3.5 E8	.020	
116	78	F	SSI TTL GATE	-	16	5	P	2.1 E7	.0044	0
178	78	G	SSI TTL GATE	7400	16	5	P	4.6 E8	.03	
104	76	C	SSI/MSI CMOS	-	13	5	H	3.6 E7	.056	20
107	76	C	SSI/MSI CMOS	-	13	5	P	3.5 E8	.029	11

TABLE .1: FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	%/1KHR	FAI
105	77	C	SSI/MSI CMOS	-	13	5	M 1.1 E8	.033	34
108	77	C	SSI/MSI CMOS	-	13	5	P 6.8 E8	.025	170
106	78	C	SSI/MSI CMOS	-	13	5	M 8.1 E7	.031	25
109	78	C	SSI/MSI CMOS	-	13	5	P 4.1 E8	.024	99
211	73	J	TRANS PWR NPN	-	10	5	P 5.6 E8	.013	68
068	76	C	TRANS PWR NPN	-	13	5	M 2.9 E8	.065	188
071	76	C	TRANS PWR NPN	-	13	5	P 1.9 E8	.077	146
123	76	G	TRANS PWR NPN	T1P31A	16	5	P 6.2 E6	.022	
126	76	G	TRANS PWR NPN	T1P47	16	5	P 1.6E7	.053	
069	77	C	TRANS PWR NPN	-	13	5	M 6.0 E8	.066	390
072	77	C	TRANS PWR NPN	-	13	5	P 3.8 E8	.065	246
124	77	G	TRANS PWR NPN	T1P31A	16	5	P 1.2 E7	.059	
127	77	G	TRANS PWR NPN	T1P47	16	5	P 1.5 E7	.23	
070	78	C	TRANS PWR NPN	-	13	5	M 2.8 E8	.098	274
073	78	C	TRANS PWR NPN	-	13	5	P 1.7 E8	.050	87
125	78	G	TRANS PWR NPN	T1P31A	16	5	P 1.2 E7	.069	
128	78	G	TRANS PWR NPN	T1P47	16	5	P 2.5 E7	.127	
212	73	J	TRANS PWR PNP	-	16	5	P 4.5 E8	.023	100
074	76	C	TRANS PWR PNP	-	13	5	P 6.9 E8	.047	32
077	76	C	TRANS PWR PNP	-	13	5	P 9.7 E8	.058	56
035	77	B	TRANS PWR PNP	2N174	17	7	M 3.6 E9	.03	
075	77	C	TRANS PWR PNP	-	13	5	M 1.5 E8	.055	131
078	77	C	TRANS PWR PNP	-	13	5	P 2.0 E8	.034	68
076	78	C	TRANS PWR PNP	-	13	5	M 7.3 E8	.060	44
079	78	C	TRANS PWR PNP	-	13	5	P 1.1 E8	.036	38
056	76	C	TRANS SS NFET	-	13	5	M 3.37 E8	.028	94
059	76	C	TRANS SS NFET	-	13	5	P 2.1 E8	.081	173
147	76	G	TRANS SS NFET	-	16	5	P 1.1 E8	.131	
150	76	G	TRANS SS NFET	-	16	5	M 8.0 E6	.032	
057	77	C	TRANS SS NFET	-	13	5	M 7.0 E8	.051	356
060	77	C	TRANS SS NFET	-	13	5	P 4.0 E8	.086	339
148	77	G	TRANS SS NFET	-	16	5	P 1.2 E6	.126	
151	77	G	TRANS SS NFET	-	16	5	M 2.0 E7	.065	
058	78	C	TRANS SS NFET	-	13	5	M 4.1 E8	.044	182
061	78	C	TRANS SS NFET	-	13	5	P 2.0 E8	.076	152
149	78	G	TRANS SS NFET	-	16	5	P 1.6 E8	.075	
152	78	G	TRANS SS NFET	-	16	5	M 2.1 E7	.026	
210	73	J	TRANS SS NPN	-	16	5	P 4.6 E9	.010	456
044	76	C	TRANS SS NPN	-	13	5	M 1.44 E9	.025	355
047	76	C	TRANS SS NPN	-	13	5	P 3.6 E9	.017	598
135	76	G	TRANS SS NPN	2N2222	16	5	M 5.3 E7	.022	
138	76	G	TRANS SS NPN	2N2219	16	5	M 7.2 E7	.096	
141	76	G	TRANS SS NPN	2N3439	16	5	M 7.8 E7	.129	
159	76	G	TRANS SS NPN	2N3904	16	5	P 1.4 E9	.024	
188	76	G	TRANS SS NPN	2N5551	16	5	P 3.2 E8	.085	
195	76	H	TRANS SS NPN	-	17	5	P 2.9 E9	.0045	
036	77	B	TRANS SS NPN	-	17	7	P 2 E9	.01	
045	77	C	TRANS SS NPN	-	13	5	M 2.92 E9	.024	703
048	77	C	TRANS SS NPN	-	13	5	P 7.0 E9	.016	1093
136	77	G	TRANS SS NPN	2N2222	16	5	M 7.0 E7	.0215	
139	77	G	TRANS SS NPN	2N2219	16	5	M 8.0 E7	.043	

TABLE 1: FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F
142	77	G	TRANS SS NPN	2N3439	16	5	H	8.2 E7	.098	
160	77	G	TRANS SS NPN	2N3904	16	5	P	1.8 E9	.020	
189	77	G	TRANS SS NPN	2N5551	16	5	P	4.0 E8	.080	
201	77	H	TRANS SS NPN	-	17	5	P	1.3 E8	.0026	6
046	78	C	TRANS SS NPN	-	13	5	H	1.6 E9	.025	396
049	78	C	TRANS SS NPN	-	13	5	P	3.6 E9	.013	468
137	78	G	TRANS SS NPN	2N2222	16	5	H	9.4 E8	.019	
140	78	G	TRANS SS NPN	2N2219	16	5	H	1.0 E8	.03	
143	78	G	TRANS SS NPN	2N3439	16	5	H	1.0 E8	.105	
161	78	G	TRANS SS NPN	2N3904	16	5	P	2.3 E9	.015	
190	78	G	TRANS SS NPN	2N5551	16	5	P	5.0 E8	.063	
062	76	C	TRANS SS PFET	-	13	5	H	1.9 E7	.005	0
065	76	C	TRANS SS PFET	-	13	5	P	9.2 E7	.031	29
063	77	C	TRANS SS PFET	-	13	5	H	1.4 E7	.030	2
066	77	C	TRANS SS PFET	-	13	5	P	1.1 E8	.033	35
064	78	C	TRANS SS PFET	-	13	5	H	7.9 E6	.012	0
067	78	C	TRANS SS PFET	-	13	5	P	5.5 E7	.042	23
213	73	J	TRANS SS PNP	-	16	5	P	3.6 E8	.029	102
050	76	C	TRANS SS PNP	-	13	5	H	1.2 E9	.027	315
053	76	C	TRANS SS PNP	-	13	5	P	2.4 E9	.023	550
051	77	C	TRANS SS PNP	-	13	5	H	2.3 E9	.026	585
054	77	C	TRANS SS PNP	-	13	5	P	5.0 E9	.021	1041
202	77	H	TRANS SS PNP	-	17	5	P	.3 E8	.0026	6
052	78	C	TRANS SS PNP	-	13	5	H	1.1 E9	.025	28
055	78	C	TRANS SS PNP	-	13	5	P	2.7 E9	.017	46
196	76	H	TRAN SS PNP	-	17	5	P	2.9 E9	.0045	

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
001	74	A	SSI TTL	-	16	5	P	1.5 E7	.042	5
002	74	A	SSI STTL	-	16	5	P	1.9 E7	.0049	0
003	74	A	SSI HTTL	-	16	5	P	1.3 E8	.013	15
004	74	A	MSI TTL	-	16	5	P	9.6 E7	.025	22
005	74	A	MSI STTL	-	16	5	P	2.2 E7	.039	7
005	74	A	MSI HTTL	-	16	5	P	5.1 E6	.018	0
007	74	A	LSI LINEAR	-	16	5	P	1.6 E6	.058	0
008	74	A	LSI STTL	-	16	5	P	1.6 E6	.058	0
009	74	A	SSI TTL	-	16	5	H	2.3 E6	.04	0
010	74	A	SSI STTL	-	16	5	H	3.6 E6	.026	0
011	74	A	SSI HTTL	-	16	5	H	2.0 E7	.0045	0
012	74	A	MSI TTL	-	16	5	H	1.5 E7	.014	1
013	74	A	MSI STTL	-	16	5	H	3.3 E6	.028	0
014	74	A	MSI HTTL	-	16	5	H	8.0 E5	.25	1
015	74	A	LSI LINEAR	-	16	5	H	2.4 E5	-	0
016	74	A	LSI STTL	-	16	5	H	3.2 E6	.025	0
017	74	A	LSI NMOS	-	16	5	H	9.3 E5	-	0
018	74	A	SSI TTL	-	16	5	P	1.3 E8	.005	5
019	74	A	SSI STTL	-	16	5	P	1.1 E8	.0029	2
020	74	A	SSI HTTL	-	16	5	P	7 E8	.003	19
021	74	A	MSI TTL	-	16	5	P	7.3 E8	.0076	53
022	74	A	MSI STTL	-	16	5	P	1.1 E8	.0076	7
023	74	A	MSI HTTL	-	16	5	P	2.3 E7	.027	5
024	74	A	LSI LINEAR	-	16	5	P	7.4 E6	.012	0
025	74	A	LSI STTL	-	16	5	P	9.6 E6	.044	3
026	74	A	SSI TTL	-	16	5	H	1.9 E7	.005	0
027	74	A	SSI STTL	-	16	5	H	1.6 E7	.006	0
028	74	A	SSI HTTL	-	16	5	H	1.1 E8	.0006	0
029	74	A	MSI TTL	-	16	5	H	1.1 E8	.0008	0
030	74	A	MSI STTL	-	16	5	H	1.7 E7	.0055	0
031	74	A	MSI HTTL	-	11	5	H	3.5 E6	.026	0
032	74	A	LSI LINEAR	-	16	5	H	1.1 E6	.082	0
033	74	A	LSI STTL	-	16	5	H	1.4 E6	.063	0
034	74	A	LSI NMOS	-	16	5	H	4.2 E6	.022	0
035	77	B	TRANS PWR PNP	2N174	17	7	H	3.6 E9	.03	
036	77	B	TRANS SS NPN	-	17	7	P	2 E9	.01	
037	77	B	DIODE SS	-	17	7	P	2.8 E9	.0074	
038	77	B	DIODE LED	-	17	7	P	2.7 E6	.012	
039	77	B	LSI PMOS	-	17	8	P	0.5 E6	.25	
040	78	B	LSI PMOS	-	17	8	P	0.5 E6	.016	
041	77	B	SSI LN OP AMP	-	17	7	P	8.1 E9	.05	
042	77	B	SSI LN VLT RG FIX	-	17	7	P	2.2 E9	.11	
043	77	B	SSI LN AM PWR	-	17	7	P	4 E7	.05	
044	76	C	TRANS SS NPN	-	13	5	H	1.44 E9	.025	355
045	77	C	TRANS SS NPN	-	13	5	H	2.92 E9	.024	703
046	78	C	TRANS SS NPN	-	13	5	H	1.6 E9	.025	396
047	76	C	TRANS SS NPN	-	13	5	P	3.6 E9	.017	596
048	77	C	TRANS SS NPN	-	13	5	P	7.0 E9	.016	1093
049	78	C	TRANS SS NPN	-	13	5	P	3.6 E9	.013	468
050	76	C	TRANS SS PNP	-	13	5	H	1.2 E9	.027	315
051	77	C	TRANS SS PNP	-	13	5	H	2.3 E9	.026	585

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	%/1KHR	F	S
052	78	C	TRANS SS PNP	-	13	5	H 1.1 E9	.025	280	
053	76	C	TRANS SS PNP	-	13	5	P 2.4 E9	.023	550	
054	77	C	TRANS SS PNP	-	13	5	P 5.0 E9	.021	1041	
055	78	C	TRANS SS PNP	-	13	5	P 2.7 E9	.017	460	
056	76	C	TRANS SS NFET	-	13	5	H 3.37 E8	.028	94	
057	77	C	TRANS SS NFET	-	13	5	H 7.0 E8	.051	356	
058	78	C	TRANS SS NFET	-	13	5	H 4.1 E8	.044	182	
059	76	C	TRANS SS NFET	-	13	5	P 2.1 E8	.081	173	
060	77	C	TRANS SS NFET	-	13	5	P 4.0 E8	.086	339	
061	78	C	TRANS SS NFET	-	13	5	P 2.0 E8	.076	152	
062	76	C	TRANS SS PFET	-	13	5	H 1.9 E7	.005	0	
063	77	C	TRANS SS PFET	-	13	5	H 1.4 E7	.030	2	
064	78	C	TRANS SS PFET	-	13	5	H 7.9 E6	.012	0	
065	76	C	TRANS SS PFET	-	13	5	P 9.2 E7	.031	29	
066	77	C	TRANS SS PFET	-	13	5	P 1.1 E8	.033	35	
067	78	C	TRANS SS PFET	-	13	5	P 5.5 E7	.042	23	
068	76	C	TRANS PWR NPN	-	13	5	H 2.9 E8	.065	188	
069	77	C	TRANS PWR NPN	-	13	5	H 6.0 E8	.066	390	
070	78	C	TRANS PWR NPN	-	13	5	H 2.8 E8	.098	274	
071	76	C	TRANS PWR NPN	-	13	5	P 1.9 E8	.077	146	
072	77	C	TRANS PWR NPN	-	13	5	P 3.8 E8	.065	246	
073	78	C	TRANS PWR NPN	-	13	5	P 1.7 E8	.050	87	
074	76	C	TRANS PWR PNP	-	13	5	P 6.9 E8	.047	32	
075	77	C	TRANS PWR PNP	-	13	5	H 1.5 E8	.055	1	
076	78	C	TRANS PWR PNP	-	13	5	H 7.3 E8	.060	44	
077	76	C	TRANS PWR PNP	-	13	5	P 9.7 E8	.058	56	
078	77	C	TRANS PWR PNP	-	13	5	P 2.0 E8	.034	68	
079	78	C	TRANS PWR PNP	-	13	5	P 1.1 E8	.036	38	
080	76	C	SSI LN OP AMP	-	13	5	H 7.7 E8	.051	393	
081	77	C	SSI LN OP AMP	-	13	5	H 1.5 E9	.050	726	
082	78	C	SSI LN OP AMP	-	13	5	H 7.7 E8	.039	304	
083	76	C	SSI LN OP AMP	-	13	5	P 8.7 E7	.008	59	
084	77	C	SSI LN OP AMP	-	13	5	P 1.8 E8	.026	139	
085	78	C	SSI LN OP AMP	-	13	5	P 1.1 E8	.022	24	
086	76	C	SSI LN VLT RG FIX	-	13	5	H 3.3 E7	.090	30	
087	77	C	SSI LN VLT RG FIX	-	13	5	H 4.5 E7	.062	50	
088	76	C	SSI LN VLT RG FIX	-	13	5	H 5.0 E7	.070	35	
089	76	C	SSI LN VLT RG FIX	-	13	5	P 4.1 E7	.092	36	
090	77	C	SSI LN VLT RG FIX	-	13	5	P 1.1 E8	.105	112	
091	78	C	SSI LN VLT RG FIX	-	13	5	P 7.4 E7	.045	33	
092	76	C	SSI LN VLT RG VAR	-	13	5	H 1.2 E8	.122	147	
093	77	C	SSI LN VLT RG VAR	-	13	5	H 2.6 E8	.112	296	
094	78	C	SSI LN VLT RG VAR	-	13	5	H 1.2 E8	.100	118	
095	76	C	SSI LN VLT RG VAR	-	13	5	P 6.3 E6	.320	20	
096	77	C	SSI LN VLT RG VAR	-	13	5	P 1.5 E7	.298	44	
097	78	C	SSI LN VLT RG VAR	-	13	5	P 1.1 E7	.140	16	
098	76	C	SSI ECL	-	13	5	H 1.7 E7	.066	11	
099	77	C	SSI ECL	-	13	5	H 6.8 E7	.038	26	
100	78	C	SSI ECL	-	13	5	H 1.0 E8	.035	35	
101	76	C	SSI ECL	-	13	5	P 9.3 E7	.041	38	
102	77	C	SSI ECL	-	13	5	P 2.5 E8	.029	70	

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
103	78	C	SSI ECL	-	13	S	P	2.5 E8	.021	51
104	76	C	SSI/MSI CMOS	-	13	S	H	3.6 E7	.056	20
105	77	C	SSI/MSI CMOS	-	13	S	H	1.1 E8	.033	34
106	78	C	SSI/MSI CMOS	-	13	S	H	8.1 E7	.031	25
107	76	C	SSI/MSI CMOS	-	13	S	P	3.5 E8	.029	101
108	77	C	SSI/MSI CMOS	-	13	S	P	6.8 E8	.025	170
109	78	C	SSI/MSI CMOS	-	13	S	P	4.1 E8	.024	99
110	73	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
111	74	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
112	75	D	LSI RAM	MODULE	12	4	C	9.2 E5	.22	1
113	73	D	LSI RAM	MODULE	12	4	C	8.7 E6	.31	25
114	74	D	LSI RAM	MODULE	12	4	C	8.8 E6	.20	17
115	78	F	SSI CMOS GATE	MEM4900P	12	S	P	8.4 E5	.24	1
116	78	F	SSI TTL GATE	-	16	S	P	2.1 E7	.0044	0
117	78	F	SSI TTL FF	-	16	S	P	5.5 E6	.017	0
118	78	F	MSI TTL GATE	-	16	S	P	7.7 E6	.012	0
119	78	F	MSI TTL FF	-	16	S	P	6.6 E6	.014	0
120	78	F	SSI LN OP AMP	-	16	S	P	3.4 E6	.027	0
121	78	F	LSI NMOS RAM	-	16	S	P	3.3 E6	.028	0
122	78	F	LSI BIPOLAR PROM	-	16	S	P	8.4 E6	.011	0
123	76	G	TRANS PWR NPN	T1P31A	16	S	P	6.2 E6	.022	
124	77	G	TRANS PWR NPN	T1P31A	16	S	P	1.2 E7	.059	
125	78	G	TRANS PWR NPN	T1P31A	16	S	P	1.2 E7	.069	
126	76	G	TRANS PWR NPN	T1P47	16	S	P	1.6E7	.053	
127	77	G	TRANS PWR NPN	T1P47	16	S	P	1.5 E7	.23	
128	78	G	TRANS PWR NPN	T1P47	16	S	P	2.5 E7	.127	
129	76	G	SSI ECL GATE	10102	16	S	H	3.9 E7	.039	
130	77	G	SSI ECL GATE	10102	16	S	H	6 E7	.031	
131	78	G	SSI ECL GATE	10102	16	S	H	7.5 E7	.039	
132	76	G	MSI ECL	10102	16	S	H	2.9 E7	.10	
133	77	G	MSI ECL	10102	16	S	H	7.2 E7	.033	
134	78	G	MSI ECL	10102	16	S	H	7.8 E7	.044	
135	76	G	TRANS SS NPN	2N2222	16	S	H	5.3 E7	.022	
136	77	G	TRANS SS NPN	2N2222	16	S	H	7.0 E7	.0215	
137	78	G	TRANS SS NPN	2N2222	16	S	H	9.4 E8	.019	
138	76	G	TRANS SS NPN	2N2219	16	S	H	7.2 E7	.096	
139	77	G	TRANS SS NPN	2N2219	16	S	H	8.0 E7	.043	
140	78	G	TRANS SS NPN	2N2219	16	S	H	1.0 E8	.03	
141	76	G	TRANS SS NPN	2N3439	16	S	H	7.8 E7	.129	
142	77	G	TRANS SS NPN	2N3439	16	S	H	8.2 E7	.098	
143	78	G	TRANS SS NPN	2N3439	16	S	H	1.0 E8	.105	
144	76	G	SCR	C106B2	16	S	P	1.6 E7	.092	
145	77	G	SCR	C106B2	16	S	P	1.8 EE	.116	
146	78	G	SCR	C106B2	16	S	P	1.9 E7	.09	
147	76	G	TRANS SS NFET	-	16	S	P	1.1 E8	.131	
148	77	G	TRANS SS NFET	-	16	S	P	1.2 E8	.126	
149	78	G	TRANS SS NFET	-	16	S	P	1.3 E8	.075	
150	76	G	TRANS SS NFET	-	16	S	H	8.0 E6	.032	
151	77	G	TRANS SS NFET	-	16	S	H	2.0 E7	.065	
152	78	G	TRANS SS NFET	-	16	S	H	2.1 E7	.026	
153	76	G	SSI LN VLT RG FIX	-	16	S	P	1.47 E7	.127	

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	Z/1KHR	F.
154	77	G	SSI LN VLT RG FIX	-	16	5	P 1.7 E7	.12	
155	78	G	SSI LN VLT RG FIX	-	16	5	P 2.7 E7	.073	
156	76	G	SSI LN VLT RG VAR	-	16	5	M 4.8 E7	.175	
157	77	G	SSI LN VLT RG VAR	-	16	5	M 4.5 E7	.17	
158	78	G	SSI LN VLT RG VAR		16	5	M 5.9 E7	.124	
159	76	G	TRANS SS NPN	2N3904	16	5	P 1.4 E9	.024	
160	77	G	TRANS SS NPN	2N3904	16	5	P 1.8 E9	.020	
161	78	G	TRANS SS NPN	2N3904	16	5	P 2.3 E9	.015	
162	76	G	SSI LN OP AMP	LM741	16	5	P 3 E8	.101	
163	77	G	SSI LN OP AMP	LM741	16	5	P 3 E8	.067	
164	78	G	SSI LN OP AMP	LM741	16	5	P 3.9 E8	.087	
165	76	G	LSI NMOS 1KRAM	2102	16	5	P 5.7 E7	.06	
166	77	G	LSI NMOS 1KRAM	2102	16	5	P 1.2 E8	.07	
167	78	G	LSI NMOS 1KRAM	2102	16	5	P 1.0 E8	.055	
168	76	G	LSI NMOS MPROC	UP6800	16	5	P 1.1 E7	.05	
169	77	G	LSI NMOS MPROC	UP6800	11	5	P 1.4 E7	.157	
170	76	G	SSI LSTTL GATE	74LS00	16	5	P 3.8 E7	.01	
171	77	G	SSI LSTTL GATE	74LS00	16	5	P 1.0 E8	.005	
172	78	G	SSI LSTTL GATE	74LS00	16	5	P 2 E8	.002	
173	76	G	MSI LSTTL FF	74LS74	16	5	P 3.6 E7	.013	
174	77	G	MSI LSTTL FF	74LS74	16	5	P 8 E7	.008	
175	78	G	MSI LSTTL FF	74LS74	16	5	P 2.0 E8	.008	
176	76	G	SSI TTL GATE	7400	16	5	P 3.4 E8	.021	
177	77	G	SSI TTL GATE	7400	16	5	P 3.5 E8	.020	
178	78	G	SSI TTL GATE	7400	16	5	P 4.6 E8	.03	
179	76	G	MSI TTL FF	7474	16	5	P 2.4 E8	.024	
180	77	G	MSI TTL FF	7474	16	5	P 2.3 E8	.021	
181	78	G	MSI TTL FF	7474	16	5	P 3.2 E8	.0235	
182	76	G	SSI STTL GATE	74S00	16	5	P 3.6 E7	.017	
183	77	G	SSI STTL GATE	74S00	16	5	P 4.5 E7	.018	
184	78	G	SSI STTL GATE	74S00	16	5	P 8.1 E7	.02	
185	76	G	MSI STTL FF	74S74	16	5	P 5.4 E6	.04	
186	77	G	MSI STTL FF	74S74	16	5	P 1.5 E7	.007	
187	78	G	MSI STTL FF	74S74	16	5	P 2.2 E7	.0142	
188	76	G	TRANS SS NPN	2N5551	16	5	P 3.2 E8	.085	
189	77	G	TRANS SS NPN	2N5551	16	5	P 4.0 E8	.080	
190	78	G	TRANS SS NPN	2N5551	16	5	P 5.0 E8	.063	
191	76	H	SSI CMOS	-	17	5	P 2.5 E9	.004	
192	76	H	LSI PMOS	-	17	5	P 3.6 E8	.045	
193	76	H	SSI LN OP AMP	741	17	5	P 3.6 E9	.001	
194	76	H	SSI LN OP AMP	1458	17	5	P 4.0 E9	.002	
195	76	H	TRANS SS NPN	-	17	5	P 2.9 E9	.0045	
196	76	H	TRAN SS PNP	-	17	5	P 2.9 E9	.0045	
197	76	H	DIODE SS	-	17	5	P 1.7 E10	.001	
198	77	H	SSI CMOS	-	17	5	P 5.1 E7	.0026	4
199	77	H	LSI PMOS	-	17	5	P 5.1 E7	.065	31
200	77	H	SSI LN OP AMP	1458	17	5	P 2.0 E8	.010	4
201	77	H	TRANS SS NPN	-	17	5	P 1.3 E8	.0026	6
202	77	H	TRANS SS PNP	-	17	5	P 1.3 E8	.0026	6
203	77	H	DIODE SS	-	17	5	P 8.7 E8	.0016	2P
204	73	J	DIODE PWR	-	16	5	P 1.9 E9	.0034	6[illegible]

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
205	73	J	DIODE SWITCHING	-	16	5	P	2.7 E11	.00058	1571
206	73	J	DIODE REF	-	16	5	P	5.6 E8	.062	337
207	73	J	DIODE ZENER	-	16	5	P	4.0 E8	.0018	6
208	73	J	DIODE LED	-	16	5	P	9.1 E8	.0010	8
209	73	J	DIODE BRIDGE ASSY	-	16	5	P	1.1 E8	.00089	0
210	73	J	TRANS SS NPN	-	16	5	P	4.6 E9	.010	456
211	73	J	TRANS PWR NPN	-	16	5	P	5.6 E8	.013	68
212	73	J	TRANS PWR PNP	-	16	5	P	4.5 E8	.023	100
213	73	J	TRANS SS PNP	-	16	5	P	3.6 E8	.029	102
214	73	J	PHOTO ISOLATOR	-	16	5	P	2.0 E9	.030	611
215	73	J	SSI LTTL	-	16	5	P	1.4 E10	.0047	656
216	73	J	SSI TTL	-	16	5	P	9.1 E9	.0090	807
217	73	J	MSI LTTL	-	16	5	P	3.7 E9	.006	242
218	73	J	MSI TTL	-	16	5	P	3.1 E9	.012	351
219	73	J	LSI PMOS	1404	16	5	M	2.3 E9	.011	236
220	73	J	SSI LN VLT REG	-	16	5	P	2.8 E9	.011	307
221	75	J	SSI TTL	-	12	5	P	1.02 E6	.090	0
222	75	J	MSI TTL	-	12	5	P	5.78 E6	.016	0
223	75	J	SSI STTL	-	12	5	P	1.77 E6	.052	0
224	75	J	SSI LSTTL	-	12	5	P	1.80 E7	.0051	0
225	75	J	SSI LN VLT REG	-	12	5	P	4.0 E6	.023	0
226	75	J	LSI PMOS	1404	12	5	M	4.2 E6	.022	0
227	75	J	SSI LN VLT REG	-	12	5	M	4.0 E6	.023	0
228	77	K	SSI TTL	-	11	5	P	4.9 E7	.015	0
229	77	K	SSI CMOS	-	11	5	P	4.9 E7	.017	7
230	77	RAC	LSI PMOS	-	13	7	P	2.4 E8	.029	67
231	77	RAC	SSI STTL	-	12,13	4	P	6.8 E6	.014	0
232	77	RAC	SSI LSTTL	-	12,13	4	P	1.3 E6	.07	0
233	77	RAC	SSI TTL	-	12,13	4	P	5.5 E6	.017	0
234	77	RAC	MSI STTL	-	13	4	P	1.1 E7	.019	11
235	77	RAC	MSI LSTTL	-	12,13	4	P	2.3 E7	.024	0
236	77	RAC	MSI TTL	-	13	4	P	3.2 E6	.13	3
237	77	RAC	MSI TTL	-	12	4	P	4.9 E6	.019	0
238	77	RAC	SSI STTL	-	5	6,10	M	4.4 E6	.021	0
239	77	RAC	SSI TTL	-	4	6,10	M	7.4 E7	.0027	1
240	77	RAC	SSI TTL	-	5	3	M	1.7 E7	.012	1
241	77	RAC	SSI TTL	-	6	3	M	5.6 E6	.11	5
242	77	RAC	SSI TTL	-	10	2	M	1.7 E7	.025	3
243	77	RAC	SSI TTL	-	13	7	M	2.6 E6	.036	0
244	77	RAC	MSI STTL	-	5	7,10	M	2.4 E6	.036	0
245	77	RAC	MSI TTL	-	5	3,6	M	4.8 E7	.0019	0
246	77	RAC	MSI TTL	-	6	3	M	1.3 E6	.16	1
247	77	RAC	MSI TTL	-	4	6,10	M	8.3 E7	.0011	0
248	77	RAC	MSI TTL	-	10	2,3	M	3.4 E7	.025	7
249	77	RAC	MSI TTL	-	13	7	M	1.7 E6	.054	0
250	76	RAC	MSI STTL	-	13	5	P	5.2 E7	.036	17
251	77	RAC	MSI LSTTL	25LS15	12	5	P	2.6 E6	.036	0
252	76	RAC	LSI ECL PROM	1307	13	5	P	8.8 E6	.023	1
253	76	RAC	LSI NMOS RAM	2102	13	5	P	1.2 E6	.076	0
254	77	RAC	LSI NMOS RAM	4096	13	5	P	6.4 E6	.049	2
255	76	RAC	LSI PMOS S/R	5007	13	5	P	2.5 E7	.12	28

TABLE 2: FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FA
256	71	RAC	MSI PMOS	-	13	9	P	2.6 E9	.052	1321
257	76	RAC	LSI NMOS MPROC	3850	12	9	P	4.3 E7	1.1	462
258	77	RAC	LSI NMOS MPROC	Z80	13	5	P	4.7 E6	.16	6
259	76	RAC	LSI CMOS COUNTER	4020	13	5	P	4.5 E6	.021	0
260	76	RAC	MSI STTL	3207A	13	5	H	3.5 E6	.026	0
261	76	RAC	LSI PMOS	5009	13	5	H	1.2 E7	.15	16
262	76	RAC	LSI PMOS	1013	13	5	H	1.0 E7	.11	9
263	75	RAC	LSI PMOS	-	13	6	H	1.8 E7	.13	22
264	77	RAC	LSI NMOS RAM	4096	13	5	H	3.1 E6	.17	4
265	72	SBM	SSI TTL	-	12	4	H	1.5 E7	.028	3
266	72	SBM	SSI TTL	-	12	4	H	9.9 E6	.054	4
267	72	SBM	SSI TTL	-	17	4	H	4.7 E6	.043	1
268	72	SBM	SSI TTL	-	12	4	P	3.3 E6	.028	0
269	72	SBM	SSI TTL	-	12	4	P	8.4 E6	.024	1
270	72	SBM	SSI TTL	-	17	4	P	1.5 E7	.022	2
271	77	K	SSI LIN	CUSTOM	12	8	P	5.2 E7	.0079	
272	72	SA	SSI TTL GATE	-	16	6	P	1.9 E9	.012	
273	72	SA	SSI TTL FF	-	16	6	P	3.2 E8	.022	
274	72	SA	MSI TTL GATE	-	16	6	P	1.7 E8	.023	
275	72	SA	MSI TTL FF	-	16	6	P	5.6 E8	.022	
276	72	SA	SSI LIN	-	16	6	P	1.6 E7	.028	
277	72	SA	LSI PMOS ROM	-	16	6	P	5 E7	.0078	
278	72	SA	LSI PMOS CHAR GEN	-	16	6	P	8.22E6	.029	
279	72	SA	LSI PMOS S/R	-	16	6	P	1.6 E7	.041	
280	72	SA	LSI PMOS RAM	-	16	6	P	5.0 E8	.019	
281	72	SA	LSI BIPOLAR RAM	-	16	6	P	4.1 E6	.126	

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APPENDIX D

TABULATION OF THE FIELD RELIABILITY DATA

TABLE OF CONTENTS

TABULATION OF THE DATA

The data gathered from the users of plastic encapsulated semiconductors described in the body of this report were tabulated in a single listing for analysis on a year-by-year basis. The listing was first arranged in order of user as shown in Table D-1. The line number is a convenient key for location of any specific entry. The year that the part was made is indicated by "YR". The source of the data is indicated in the "SRC" column which lists the codes for the various user. The next column is the general classification of the parts, basically following the designations indicated in Table 2. (see page 11) Where the part number was known, it is entered in the "PART #" column. In many cases, the data covered a variety of different part numbers and the specific part number for the entry could not be listed. The "SCR" column identifies the screen tnat the parts received prior to installation in the operating equipment, and the "ENV" column defines the operating environment seen by the parts. The codes for these two columns are defined in Table 5. (Page 16) The type of device package is defined in the "PK" column, in which P means plastic, H means hermetic, and C means ceramic with polymer sealing. The number of operating device hours is listed for each part type in the "DEV HRS" column which uses the exponential notation to represent the decimal multiplier (e.g., 1.5 E7 means 1.5×10^7). The failure rate of the part type is given in percent per 1000 hours, and the number of parts that failed is listed in the "FAILS" column when it was known.

To facilitate the plotting of the failure rates as a function of time for each of the part types, a re-sort was made of the data listing so as to list the data by part classification. Table D-2 gives the same data as Table D-1, but here the data are arranged first by part classification and then by year.

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
001	74	A	SSI TTL	-	16	5	P	1.5 E7	.042	5
002	74	A	SSI STTL	-	16	5	P	1.9 E7	.0049	0
003	74	A	SSI HTTL	-	16	5	P	1.3 E8	.013	15
004	74	A	MSI TTL	-	16	5	P	9.6 E7	.025	22
005	74	A	MSI STTL	-	16	5	P	2.2 E7	.039	7
005	74	A	MSI HTTL	-	16	5	P	5.1 E6	.018	0
007	74	A	LSI LINEAR	-	16	5	P	1.6 E6	.058	0
008	74	A	LSI STTL	-	16	5	P	1.0 E6	.058	0
009	74	A	SSI TTL	-	16	5	M	2.3 E6	.04	0
010	74	A	SSI STTL	-	16	5	M	3.0 E6	.026	0
011	74	A	SSI HTTL	-	16	5	M	2.0 E7	.0045	0
012	74	A	MSI TTL	-	16	5	M	1.5 E7	.014	1
013	74	A	MSI STTL	-	16	5	M	3.3 E6	.028	0
014	74	A	MSI HTTL	-	16	5	M	8.0 E5	.25	1
015	74	A	LSI LINEAR	-	16	5	M	2.4 E5	-	0
016	74	A	LSI STTL	-	16	5	M	3.2 E6	.025	0
017	74	A	LSI NMOS	-	16	5	M	9.3 E5	-	0
018	74	A	SSI TTL	-	16	5	P	1.3 E8	.005	5
019	74	A	SSI STTL	-	16	5	P	1.1 E8	.0029	2
020	74	A	SSI HTTL	-	16	5	P	7 E8	.003	19
021	74	A	MSI TTL	-	16	5	P	7.3 E8	.0076	53
022	74	A	MSI STTL	-	16	5	P	1.1 E8	.0076	7
023	74	A	MSI HTTL	-	16	5	P	2.3 E7	.027	5
024	74	A	LSI LINEAR	-	16	5	P	7.4 E6	.012	0
025	74	A	LSI STTL	-	16	5	P	9.6 E6	.044	3
026	74	A	SSI TTL	-	16	5	M	1.9 E7	.005	0
027	74	A	SSI STTL	-	16	5	M	1.6 E7	.006	0
028	74	A	SSI HTTL	-	16	5	M	1.1 E8	.0008	0
029	74	A	MSI TTL	-	16	5	M	1.1 E8	.0008	0
030	74	A	MSI STTL	-	16	5	M	1.7 E7	.0055	0
031	74	A	MSI HTTL	-	11	5	M	3.5 E6	.026	0
032	74	A	LSI LINEAR	-	16	5	M	1.1 E6	.082	0
033	74	A	LSI STTL	-	16	5	M	1.4 E6	.063	0
034	74	A	LSI NMOS	-	16	5	M	4.2 E6	.022	0
035	77	B	TRANS PWR PNP	2N174	17	7	M	3.0 E9	.03	
036	77	B	TRANS SS NPN	-	17	7	P	2 E9	.01	
037	77	B	DIODE SS	-	17	7	P	2.8 E9	.0074	
038	77	B	DIODE LED	-	17	7	P	2.7 E6	.012	
039	77	B	LSI PMOS	-	17	8	P	0.5 E6	.25	
040	78	B	LSI PMOS	-	17	8	P	0.5 E6	.016	
041	77	B	SSI LN OP AMP	-	17	7	P	8.1 E9	.05	
042	77	B	SSI LN VLT RG FIX	-	17	7	P	2.2 E9	.11	
043	77	B	SSI LN AM PWR	-	17	7	P	4 E7	.05	
044	76	C	TRANS SS NPN	-	13	5	M	1.44 E9	.025	355
045	77	C	TRANS SS NPN	-	13	5	M	2.92 E9	.024	703
046	78	C	TRANS SS NPN	-	13	5	M	1.6 E9	.025	396
047	76	C	TRANS SS NPN	-	13	5	P	3.6 E9	.017	598
048	77	C	TRANS SS NPN	-	13	5	P	7.0 E9	.016	1093
049	78	C	TRANS SS NPN	-	13	5	P	3.0 E9	.013	408
050	76	C	TRANS SS PNP	-	13	5	M	1.2 E9	.027	315
051	77	C	TRANS SS PNP	-	13	5	M	2.3 E9	.026	585

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	%/1KHR	FI
052	78	C	TRANS SS PNP	-	13	5	H 1.1 E9	.025	280
053	76	C	TRANS SS PNP	-	13	5	P 2.4 E9	.023	550
054	77	C	TRANS SS PNP	-	13	5	P 5.0 E9	.021	1041
055	78	C	TRANS SS PNP	-	13	5	P 2.7 E9	.017	460
056	76	C	TRANS SS NFET	-	13	5	H 3.37 E8	.028	94
057	77	C	TRANS SS NFET	-	13	5	H 7.0 E8	.051	356
058	78	C	TRANS SS NFET	-	13	5	H 4.1 E8	.044	182
059	76	C	TRANS SS NFET	-	13	5	P 2.1 E8	.081	173
060	77	C	TRANS SS NFET	-	13	5	P 4.0 E8	.086	339
061	78	C	TRANS SS NFET	-	13	5	P 2.0 E8	.076	152
062	76	C	TRANS SS PFET	-	13	5	H 1.9 E7	.005	0
063	77	C	TRANS SS PFET	-	13	5	H 1.4 E7	.030	2
064	78	C	TRANS SS PFET	-	13	5	H 7.9 E6	.012	0
065	76	C	TRANS SS PFET	-	13	5	P 9.2 E7	.031	29
066	77	C	TRANS SS PFET	-	13	5	P 1.1 E8	.033	35
067	78	C	TRANS SS PFET	-	13	5	P 5.5 E7	.042	23
068	76	C	TRANS PWR NPN	-	13	5	H 2.9 E8	.065	188
069	77	C	TRANS PWR NPN	-	13	5	H 6.0 E8	.066	390
070	78	C	TRANS PWR NPN	-	13	5	H 2.8 E8	.098	274
071	76	C	TRANS PWR NPN	-	13	5	P 1.9 E8	.077	146
072	77	C	TRANS PWR NPN	-	13	5	P 3.8 E8	.065	246
073	78	C	TRANS PWR NPN	-	13	5	P 1.7 E8	.050	87
074	76	C	TRANS PWR PNP	-	13	5	P 6.9 E8	.047	32
075	77	C	TRANS PWR PNP	-	13	5	H 1.5 E8	.055	13
076	78	C	TRANS PWR PNP	-	13	5	H 7.3 E8	.060	4
077	76	C	TRANS PWR PNP	-	13	5	P 9.7 E8	.058	56
078	77	C	TRANS PWR PNP	-	13	5	P 2.0 E8	.034	68
079	78	C	TRANS PWR PNP	-	13	5	P 1.1 E8	.036	38
080	76	C	SSI LN OP AMP	-	13	5	H 7.7 E8	.051	393
081	77	C	SSI LN OP AMP	-	13	5	H 1.5 E9	.050	726
082	78	C	SSI LN OP AMP	-	13	5	H 7.7 E8	.059	304
083	76	C	SSI LN OP AMP	-	13	5	P 3.7 E7	.008	59
084	77	C	SSI LN OP AMP	-	13	5	P 1.8 E8	.026	139
085	78	C	SSI LN OP AMP	-	13	5	P 1.1 E8	.022	24
086	76	C	SSI LN VLT RG FIX	-	13	5	H 3.3 E7	.090	30
087	77	C	SSI LN VLT RG FIX	-	13	5	H 4.5 E7	.062	50
088	76	C	SSI LN VLT RG FIX	-	13	5	H 5.0 E7	.070	35
089	76	C	SSI LN VLT RG FIX	-	13	5	P 4.1 E7	.092	38
090	77	C	SSI LN VLT RG FIX	-	13	5	P 1.1 E8	.103	112
091	78	C	SSI LN VLT RG FIX	-	13	5	P 7.4 E7	.045	33
092	76	C	SSI LN VLT RG VAR	-	13	5	H 1.2 E8	.122	147
093	77	C	SSI LN VLT RG VAR	-	13	5	H 2.6 E8	.112	296
094	78	C	SSI LN VLT RG VAR	-	13	5	H 1.2 E8	.100	118
095	76	C	SSI LN VLT RG VAR	-	13	5	P 6.5 E6	.520	20
096	77	C	SSI LN VLT RG VAR	-	13	5	P 1.5 E7	.298	44
097	78	C	SSI LN VLT RG VAR	-	13	5	P 1.1 E7	.140	16
098	76	C	SSI ECL	-	13	5	H 1.7 E7	.000	11
099	77	C	SSI ECL	-	13	5	H 6.8 E7	.056	20
100	78	C	SSI ECL	-	13	5	H 1.0 E8	.035	35
101	76	C	SSI ECL	-	13	5	P 9.3 E7	.041	38
102	77	C	SSI ECL	-	13	5	P 2.5 E8	.029	7

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PR	DEV HRS	%/1KHR	FA
103	78	C	SSI ECL	-	13	S	P	2.5 E8	.021	51
104	76	C	SSI/MSI CMOS	-	13	S	M	3.6 E7	.056	20
105	77	C	SSI/MSI CMOS	-	13	S	M	1.1 E8	.033	34
106	78	C	SSI/MSI CMOS	-	13	S	M	6.1 E7	.031	25
107	76	C	SSI/MSI CMOS	-	13	S	P	3.5 E8	.029	10
108	77	C	SSI/MSI CMOS	-	13	S	P	6.8 E8	.025	17
109	78	C	SSI/MSI CMOS	-	13	S	P	4.1 E8	.024	99
110	73	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
111	74	D	LSI RAM	MODULE	12	4	C	1.5 E6	.062	0
112	75	D	LSI RAM	MODULE	12	4	C	9.2 E5	.22	1
113	73	D	LSI RAM	MODULE	12	4	C	8.7 E6	.31	25
114	74	D	LSI RAM	MODULE	12	4	C	8.8 E6	.20	17
115	78	F	SSI CMOS GATE	MEM4900P	12	S	P	8.4 E5	.24	1
116	78	F	SSI TTL GATE	-	16	S	P	2.1 E7	.0044	0
117	78	F	SSI TTL FF	-	16	S	P	5.5 E6	.017	0
118	78	F	MSI TTL GATE	-	16	S	P	7.7 E6	.012	0
119	78	F	MSI TTL FF	-	16	S	P	6.6 E6	.014	0
120	78	F	SSI LN OP AMP	-	16	S	P	3.4 E6	.027	0
121	78	F	LSI NMOS RAM	-	16	S	P	3.3 E6	.028	0
122	78	F	LSI BIPOLAR PROM	-	16	S	P	8.4 E5	.011	0
123	76	G	TRANS PWR NPN	T1P31A	16	S	P	6.2 E6	.022	
124	77	G	TRANS PWR NPN	T1P31A	16	S	P	1.2 E7	.059	
125	78	G	TRANS PWR NPN	T1P31A	16	S	P	1.2 E7	.069	
126	76	G	TRANS PWR NPN	T1P47	16	S	P	1.6E7	.053	
127	77	G	TRANS PWR NPN	T1P47	16	S	P	1.5 E7	.23	
128	78	G	TRANS PWR NPN	T1P47	16	S	P	2.5 E7	.127	
129	76	G	SSI ECL GATE	10102	16	S	M	3.9 E7	.039	
130	77	G	SSI ECL GATE	10102	16	S	M	6 E7	.031	
131	78	G	SSI ECL GATE	10102	16	S	M	7.5 E7	.039	
132	76	G	MSI ECL	10102	16	S	M	2.9 E7	.10	
133	77	G	MSI ECL	10102	16	S	M	7.2 E7	.033	
134	78	G	MSI ECL	10102	16	S	M	7.8 E7	.044	
135	76	G	TRANS SS NPN	2N2222	16	S	M	5.3 E7	.022	
136	77	G	TRANS SS NPN	2N2222	16	S	M	7.0 E7	.0215	
137	78	G	TRANS SS NPN	2N2222	16	S	M	9.4 E8	.019	
138	76	G	TRANS SS NPN	2N2219	16	S	M	7.2 E7	.096	
139	77	G	TRANS SS NPN	2N2219	16	S	M	6.0 E7	.043	
140	78	G	TRANS SS NPN	2N2219	16	S	M	1.0 E8	.03	
141	76	G	TRANS SS NPN	2N3439	16	S	M	7.8 E7	.129	
142	77	G	TRANS SS NPN	2N3439	16	S	M	8.2 E7	.098	
143	78	G	TRANS SS NPN	2N3439	16	S	M	1.0 E8	.105	
144	76	G	SCR	C106B2	16	S	P	1.6 E7	.062	
145	77	G	SCR	C106B2	16	S	P	1.8 EE	.116	
146	78	G	SCR	C106B2	16	S	P	1.9 E7	.09	
147	76	G	TRANS SS NFET	-	16	S	P	1.1 E8	.131	
148	77	G	TRANS SS NFET	-	16	S	P	1.2 E8	.126	
149	78	G	TRANS SS NFET	-	16	S	P	1.6 E8	.075	
150	76	G	TRANS SS NFET	-	16	S	M	6.0 E6	.052	
151	77	G	TRANS SS NFET	-	16	S	M	2.0 E7	.065	
152	78	G	TRANS SS NFET	-	16	S	M	2.1 E7	.026	
153	76	G	SSI LN VLT RG FIX	-	16	S	P	1.47 E7	.127	

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F/
154	77	G	SSI LN VLT RG FIX	-	1o	5	P	1.7 E7	.12	
155	78	G	SSI LN VLT RG FIX	-	16	5	P	2.7 E7	.073	
156	7o	G	SSI LN VLT RG VAR	-	16	5	H	4.8 E7	.175	
157	77	G	SSI LN VLT RG VAR	-	1o	5	H	4.5 E7	.17	
158	78	G	SSI LN VLT RG VAR		1o	5	H	5.9 E7	.124	
159	76	G	TRANS SS NPN	2N3904	1o	5	P	1.4 E9	.024	
160	77	G	TRANS SS NPN	2N3904	16	5	P	1.8 E9	.020	
161	78	G	TRANS SS NPN	2N3904	1o	5	P	2.3 E9	.015	
162	7o	G	SSI LN OP AMP	LM741	1o	5	P	3 E8	.101	
163	77	G	SSI LN OP AMP	LM741	1o	5	P	3 E8	.067	
164	75	G	SSI LN OP AMP	LM741	1o	5	P	5.9 E8	.087	
165	7o	G	LSI NMOS 1KRAM	2102	1o	5	P	5.7 E7	.o6	
166	77	G	LSI NMOS 1KRAM	2102	1o	5	P	1.2 E8	.07	
167	78	G	LSI NMOS 1KRAM	2102	1o	5	P	1.0 E8	.055	
168	7o	G	LSI NMOS MPROC	UP6800	1o	5	P	1.1 E7	.05	
169	77	G	LSI NMOS MPROC	UP6800	11	5	P	1.4 E7	.157	
170	7o	G	SSI LSTTL GATE	74LS00	1o	5	P	3.8 E7	.01	
171	77	G	SSI LSTTL GATE	74LS00	1o	5	P	1.0 E8	.005	
172	78	G	SSI LSTTL GATE	74LS00	1o	5	P	2 E8	.002	
173	7o	G	MSI LSTTL FF	74LS74	16	5	P	3.6 E7	.013	
174	77	G	MSI LSTTL FF	74LS74	1o	5	P	8 E7	.008	
175	78	G	MSI LSTTL FF	74LS74	1o	5	P	2.0 E8	.008	
176	76	G	SSI TTL GATE	7400	1o	5	P	3.4 E8	.021	
177	77	G	SSI TTL GATE	7400	1o	5	P	3.5 E8	.020	
178	78	G	SSI TTL GATE	7400	1o	5	P	4.6 E8	.03	
179	76	G	MSI TTL FF	7474	1o	5	P	2.4 E8	.024	
180	77	G	MSI TTL FF	7474	1o	5	P	2.3 E8	.021	
181	78	G	MSI TTL FF	7474	1o	5	P	3.2 E8	.0235	
182	7o	G	SSI STTL GATE	74S00	1o	5	P	3.o E7	.017	
183	77	G	SSI STTL GATE	74S00	1o	5	P	4.5 E7	.018	
184	78	G	SSI STTL GATE	74S00	16	5	P	8.1 E7	.02	
185	7o	G	MSI STTL FF	74S74	1o	5	P	5.4 Eo	.04	
186	77	G	MSI STTL FF	74S74	1o	5	P	1.5 E7	.007	
187	78	G	MSI STTL FF	74S74	1o	5	P	2.2 E7	.0142	
188	7o	G	TRANS SS NPN	2N5551	16	5	P	3.2 E8	.085	
189	77	G	TRANS SS NPN	2N5551	1o	5	P	4.0 E8	.080	
190	78	G	TRANS SS NPN	2N5551	1o	5	P	5.0 E8	.063	
191	7o	H	SSI CMOS	-	17	5	P	2.5 E9	.004	
192	7o	H	LSI PMOS	-	17	5	P	3.o E8	.045	
193	7o	H	SSI LN OP AMP	741	17	5	P	3.o E9	.001	
194	7o	H	SSI LN OP AMP	1458	17	5	P	4.0 E9	.002	
195	7o	H	TRANS SS NPN	-	17	5	P	2.9 E9	.0045	
196	7o	H	TRAN SS PNP	-	17	5	P	2.9 E9	.0045	
197	7o	H	DIODE SS	-	17	5	P	1.7 E10	.001	
198	77	H	SSI CMOS	-	17	5	P	5.1 E7	.002o	4
199	77	H	LSI PMOS	-	17	5	P	5.1 E7	.065	51
200	77	H	SSI LN OP AMP	1458	17	5	P	2.0 E8	.010	4
201	77	H	TRANS SS NPN	-	17	5	P	1.3 E8	.002o	o
202	77	H	TRANS SS PNP	-	17	5	P	1.3 E8	.002o	o
203	77	H	DIODE SS	-	17	5	P	8.7 E8	.001o	28
204	73	J	DIODE PAR	-	1o	5	P	1.9 E9	.0034	o2

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
205	73	J	DIODE SWITCHING	-	16	5	P	2.7 E11	.00058	1571
206	73	J	DIODE REF	-	16	5	P	5.6 E8	.062	337
207	73	J	DIODE ZENER	-	16	5	P	4.0 E8	.0018	6
208	73	J	DIODE LED	-	16	5	P	9.1 E8	.0010	8
209	73	J	DIODE BRIDGE ASSY	-	16	5	P	1.1 E8	.00089	0
210	73	J	TRANS SS NPN	-	16	5	P	4.6 E9	.010	456
211	73	J	TRANS PWR NPN	-	16	5	P	5.6 E8	.013	68
212	73	J	TRANS PWR PNP	-	16	5	P	4.5 E8	.023	100
213	73	J	TRANS SS PNP	-	16	5	P	3.6 E8	.029	102
214	73	J	PHOTO ISOLATOR	-	16	5	P	2.0 E9	.630	611
215	73	J	SSI LTTL	-	16	5	P	1.4 E10	.0047	656
216	73	J	SSI TTL	-	16	5	P	9.1 E9	.0090	807
217	73	J	MSI LTTL	-	16	5	P	3.7 E9	.066	242
218	73	J	MSI TTL	-	16	5	P	3.1 E9	.012	351
219	73	J	LSI PMOS	1404	16	5	H	2.3 E9	.011	236
220	73	J	SSI LN VLT REG	-	16	5	P	2.8 E9	.011	307
221	75	J	SSI TTL	-	12	5	P	1.02 E6	.090	0
222	75	J	MSI TTL	-	12	5	P	5.78 E6	.016	0
223	75	J	SSI STTL	-	12	5	P	1.77 E6	.052	0
224	75	J	SSI LSTTL	-	12	5	P	1.80 E7	.0051	0
225	75	J	SSI LN VLT REG	-	12	5	P	4.0 E6	.023	0
226	75	J	LSI PMOS	1404	12	5	H	4.2 E6	.022	0
227	75	J	SSI LN VLT REG	-	12	5	H	4.0 E6	.023	0
228	77	K	SSI TTL	-	11	5	P	4.9 E7	.015	6
229	77	K	SSI CMOS	-	11	5	P	4.9 E7	.017	7
230	77	RAC	LSI PMOS	-	13	7	P	2.4 E8	.029	67
231	77	RAC	SSI STTL	-	12,13	4	P	6.8 E6	.014	0
232	77	RAC	SSI LSTTL	-	12,13	4	P	1.3 E6	.07	0
233	77	RAC	SSI TTL	-	12,13	4	P	5.5 E6	.017	0
234	77	RAC	MSI STTL	-	13	4	P	1.1 E7	.019	11
235	77	RAC	MSI LSTTL	-	12,13	4	P	2.3 E7	.024	0
236	77	RAC	MSI TTL	-	13	4	P	3.2 E6	.13	3
237	77	RAC	MSI TTL	-	12	4	P	4.9 E6	.019	0
238	77	RAC	SSI STTL	-	5	6,10	H	4.4 E6	.021	0
239	77	RAC	SSI TTL	-	4	6,10	H	7.4 E7	.0027	1
240	77	RAC	SSI TTL	-	5	3	H	1.7 E7	.012	1
241	77	RAC	SSI TTL	-	6	3	H	5.8 E6	.11	5
242	77	RAC	SSI TTL	-	10	2	H	1.7 E7	.025	3
243	77	RAC	SSI TTL	-	13	7	H	2.6 E6	.036	0
244	77	RAC	MSI STTL	-	5	7,10	H	2.4 E6	.038	0
245	77	RAC	MSI TTL	-	5	3,6	H	4.8 E7	.0019	0
246	77	RAC	MSI TTL	-	6	3	H	1.3 E6	.16	1
247	77	RAC	MSI TTL	-	4	6,10	H	8.3 E7	.0011	0
248	77	RAC	MSI TTL	-	10	2,3	H	3.4 E7	.025	7
249	77	RAC	MSI TTL	-	13	7	H	1.7 E6	.054	0
250	76	RAC	MSI STTL	-	13	5	P	5.2 E7	.036	17
251	77	RAC	MSI LSTTL	25LS15	12	5	P	2.6 E6	.036	0
252	76	RAC	LSI ECL PROM	1307	13	5	P	8.8 E6	.023	1
253	76	RAC	LSI NMOS RAM	2102	13	5	P	1.2 E6	.076	0
254	77	RAC	LSI NMOS RAM	4096	13	5	P	6.4 E6	.049	2
255	76	RAC	LSI PMOS S/R	5007	13	5	P	2.5 E7	.12	28

TABLE D-1 FIELD USAGE FAILURE RATE DATA TABULATED IN USER SEQUENCE

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F
256	71	RAC	MSI PMOS	-	13	9	P	2.6 E9	.052	1321
257	76	RAC	LSI NMOS MPRUC	3850	12	9	P	4.3 E7	1.1	462
258	77	RAC	LSI NMOS MPRUC	Z80	13	5	P	4.7 E6	.16	6
259	76	RAC	LSI CMOS COUNTER	4020	13	5	P	4.5 E6	.021	0
260	76	RAC	MSI STTL	3207A	13	5	H	3.5 E6	.026	0
261	76	RAC	LSI PMOS	5009	13	5	H	1.2 E7	.15	16
262	76	RAC	LSI PMOS	1013	13	5	H	1.0 E7	.11	9
263	75	RAC	LSI PMOS	-	13	6	H	1.8 E7	.13	22
264	77	RAC	LSI NMOS RAM	4096	13	5	H	3.1 E6	.17	4
265	72	SBM	SSI TTL	-	12	4	H	1.5 E7	.028	3
266	72	SBM	SSI TTL	-	12	4	H	9.9 E6	.054	4
267	72	SBM	SSI TTL	-	17	4	H	4.7 E6	.043	1
268	72	SBM	SSI TTL	-	12	4	P	3.3 E6	.028	0
269	72	SBM	SSI TTL	-	12	4	P	8.4 E6	.024	1
270	72	SBM	SSI TTL	-	17	4	P	1.5 E7	.022	2
271	77	K	SSI LIN	CUSTOM	12	8	P	5.2 E7	.0079	
272	72	SA	SSI TTL GATE	-	16	6	P	1.9 E9	.012	
273	72	SA	SSI TTL FF	-	16	6	P	3.2 E8	.022	
274	72	SA	MSI TTL GATE	-	16	6	P	1.7 E8	.023	
275	72	SA	MSI TTL FF	-	16	6	P	5.6 E8	.022	
276	72	SA	SSI LIN	-	16	6	P	1.6 E7	.028	
277	72	SA	LSI PMOS ROM	-	16	6	P	5 E7	.0078	
278	72	SA	LSI PMOS CHAR GEN	-	16	6	P	8.22E6	.029	
279	72	SA	LSI PMOS S/R	-	16	6	P	1.6 E7	.041	
280	72	SA	LSI PMOS RAM	-	16	6	P	5.0 E8	.019	
281	72	SA	LSI BIPOLAR RAM	-	16	6	P	4.1 E6	.128	

TABLE D-2 FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	%/1KHR	FAILS
209	73	J	DIODE BRIDGE ASSY	-	16	5	P 1.1 E8	.00089	0
208	73	J	DIODE LED	-	16	5	P 9.1 E8	.0010	8
038	77	B	DIODE LED	-	17	7	P 2.7 E6	.012	
204	73	J	DIODE PWR	-	16	5	P 1.9 E9	.0034	62
206	73	J	DIODE REF	-	16	5	P 5.6 E8	.062	337
197	76	H	DIODE SS	-	17	5	P 1.7 E10	.001	
037	77	B	DIODE SS	-	17	7	P 2.8 E9	.0074	
203	77	H	DIODE SS	-	17	5	P 8.7 E8	.0016	28
205	73	J	DIODE SWITCHING	-	16	5	P 2.7 E11	.00058	1571
207	73	J	DIODE ZENER	-	16	5	P 4.0 E8	.0018	0
122	78	F	LSI BIPOLAR PROM	-	16	5	P 8.4 E6	.011	0
281	72	SA	LSI BIPOLAR RAM	-	16	6	P 4.1 E6	.128	
259	76	RAC	LSI CMOS COUNTER	4020	13	5	P 4.5 E6	.021	0
252	76	RAC	LSI ECL PROM	1307	13	5	P 8.8 E6	.023	1
007	74	A	LSI LINEAR	-	16	5	P 1.6 E5	.058	0
015	74	A	LSI LINEAR	-	16	5	H 2.4 E5	-	0
024	74	A	LSI LINEAR	-	16	5	P 7.4 E6	.012	0
032	74	A	LSI LINEAR	-	16	5	H 1.1 E6	.082	0
017	74	A	LSI NMOS	-	16	5	H 9.3 E5	-	0
034	74	A	LSI NMOS	-	16	5	H 4.2 E6	.022	0
168	76	G	LSI NMOS MPROC	UP6800	16	5	P 1.1 E7	.05	
257	76	RAC	LSI NMOS MPROC	3850	12	9	P 4.3 E7	1.1	462
169	77	G	LSI NMOS MPROC	UP6800	11	5	P 1.4 E7	.157	
258	77	RAC	LSI NMOS MPROC	Z80	13	5	P 4.7 E6	.16	0
253	76	RAC	LSI NMOS RAM	2102	13	5	P 1.2 E6	.076	0
254	77	RAC	LSI NMOS RAM	4096	13	5	P 6.4 E6	.049	2
264	77	RAC	LSI NMOS RAM	4096	13	5	H 3.1 E6	.17	4
121	78	F	LSI NMOS RAM	-	16	5	P 3.3 E6	.028	0
165	76	G	LSI NMOS 1KRAM	2102	16	5	P 5.7 E7	.06	
166	77	G	LSI NMOS 1KRAM	2102	16	5	P 1.2 E8	.07	
167	78	G	LSI NMOS 1KRAM	2102	16	5	P 1.0 E8	.055	
219	73	J	LSI PMOS	1404	16	5	H 2.3 E9	.011	236
226	75	J	LSI PMOS	1404	12	5	H 4.2 E6	.022	0
263	75	RAC	LSI PMOS	-	13	6	H 1.8 E7	.13	22
192	76	H	LSI PMOS	-	17	5	P 3.0 E8	.045	
261	76	RAC	LSI PMOS	5009	13	5	H 1.2 E7	.15	16
262	76	RAC	LSI PMOS	1013	13	5	H 1.0 E7	.11	9
039	77	B	LSI PMOS	-	17	8	P 0.5 E6	.25	
199	77	H	LSI PMOS	-	17	5	P 5.1 E7	.005	31
230	77	RAC	LSI PMOS	-	13	7	P 2.4 E8	.029	07
040	78	B	LSI PMOS	-	17	8	P 0.5 E6	.016	
278	72	SA	LSI PMOS CHAR GEN	-	16	6	P 8.22E6	.029	
280	72	SA	LSI PMOS RAM	-	16	6	P 5.0 E8	.019	
277	72	SA	LSI PMOS ROM	-	16	6	P 5 E7	.0078	
279	72	SA	LSI PMOS S/R	-	16	6	P 1.6 E7	.041	
255	76	RAC	LSI PMOS S/R	5007	13	5	P 2.5 E7	.12	28
110	73	D	LSI RAM	MODULE	12	4	C 1.5 E6	.062	0
113	73	D	LSI RAM	MODULE	12	4	C 8.7 E6	.31	25
111	74	D	LSI RAM	MODULE	12	4	C 1.5 E6	.062	0
114	74	D	LSI RAM	MODULE	12	4	C 8.8 E6	.20	17
112	75	D	LSI RAM	MODULE	12	4	C 9.2 E5	.22	1

TABLE D-2 FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	F.
008	74	A	LSI STTL	-	16	5	P	1.5 E6	.058	0
016	74	A	LSI STTL	-	16	5	M	3.2 E6	.025	0
025	74	A	LSI STTL	-	16	5	P	9.6 E6	.044	3
033	74	A	LSI STTL	-	16	5	M	1.4 E6	.063	0
132	76	G	MSI ECL	10102	16	5	M	2.9 E7	.10	
133	77	G	MSI ECL	10102	16	5	M	7.2 E7	.033	
134	78	G	MSI ECL	10102	16	5	M	7.8 E7	.044	
005	74	A	MSI HTTL	-	16	5	P	5.1 E6	.018	0
014	74	A	MSI HTTL	-	16	5	M	8.0 E5	.25	1
023	74	A	MSI HTTL	-	16	5	P	2.3 E7	.027	5
031	74	A	MSI HTTL	-	11	5	M	3.5 E6	.026	0
235	77	RAC	MSI LSTTL	-	12,13	4	P	2.3 E7	.024	0
251	77	RAC	MSI LSTTL	25LS15	12	5	P	2.6 E6	.036	0
173	76	G	MSI LSTTL FF	74LS74	16	5	P	3.6 E7	.013	
174	77	G	MSI LSTTL FF	74LS74	16	5	P	8 E7	.008	
175	78	G	MSI LSTTL FF	74LS74	16	5	P	2.0 E8	.008	
217	73	J	MSI LTTL	-	16	5	P	3.7 E9	.006	242
250	71	RAC	MSI PMOS	-	13	9	P	2.6 E9	.052	1321
005	74	A	MSI STTL	-	16	5	P	2.2 E7	.039	7
013	74	A	MSI STTL	-	16	5	M	3.3 E6	.028	0
022	74	A	MSI STTL	-	16	5	P	1.1 E8	.0076	7
030	74	A	MSI STTL	-	16	5	M	1.7 E7	.0055	0
250	76	RAC	MSI STTL	-	13	5	P	5.2 E7	.036	17
260	76	RAC	MSI STTL	3207A	13	5	M	3.5 E6	.026	0
234	77	RAC	MSI STTL	-	13	4	P	1.1 E7	.019	1
244	77	RAC	MSI STTL	-	5	7,10	M	2.4 E6	.038	0
185	76	G	MSI STTL FF	74S74	16	5	P	5.4 E6	.04	
186	77	G	MSI STTL FF	74S74	16	5	P	1.5 E7	.007	
187	78	G	MSI STTL FF	74S74	16	5	P	2.2 E7	.0142	
218	73	J	MSI TTL	-	16	5	P	3.1 E9	.012	351
004	74	A	MSI TTL	-	16	5	P	9.6 E7	.025	22
012	74	A	MSI TTL	-	16	5	M	1.5 E7	.014	1
021	74	A	MSI TTL	-	16	5	P	7.3 E8	.0076	55
029	74	A	MSI TTL	-	16	5	M	1.1 E8	.0008	0
222	75	J	MSI TTL	-	12	5	P	5.78 E6	.016	0
236	77	RAC	MSI TTL	-	13	4	P	3.2 E6	.13	3
237	77	RAC	MSI TTL	-	12	4	P	4.9 E6	.019	0
245	77	RAC	MSI TTL	-	5	5,6	M	4.8 E7	.0019	0
246	77	RAC	MSI TTL	-	6	3	M	1.3 E6	.16	1
247	77	RAC	MSI TTL	-	4	6,10	M	8.3 E7	.0011	0
248	77	RAC	MSI TTL	-	10	2,3	M	3.4 E7	.025	7
249	77	RAC	MSI TTL	-	13	7	M	1.7 E6	.054	0
275	72	SA	MSI TTL FF	-	16	6	P	5.6 E8	.022	
179	76	G	MSI TTL FF	7474	16	5	P	2.4 E8	.024	
180	77	G	MSI TTL FF	7474	16	5	P	2.3 E8	.021	
119	78	F	MSI TTL FF	-	16	5	P	6.6 E6	.014	0
181	78	G	MSI TTL FF	7474	16	5	P	3.2 E8	.0255	
274	72	SA	MSI TTL GATE	-	16	6	P	1.7 E8	.023	
118	78	F	MSI TTL GATE	-	16	5	P	7.7 E6	.012	0
214	73	J	PHOTO ISOLATOR	-	16	5	P	2.0 E9	.030	61
144	76	G	SCR	C10682	16	5	P	1.6 E7	.042	

TABLE D-2 FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FAILS
145	77	G	SCR	C10682	10	5	P	1.8 EE	.110	
146	78	G	SCR	C10682	10	5	P	1.9 E7	.09	
191	76	H	SSI CMOS	-	17	5	P	2.5 E9	.004	
198	77	H	SSI CMOS	-	17	5	P	5.1 E7	.0026	4
229	77	K	SSI CMOS	-	11	5	P	4.9 E7	.017	7
115	78	F	SSI CMOS GATE	MEM4900P	12	5	P	8.4 E5	.24	1
098	76	C	SSI ECL	-	13	5	M	1.7 E7	.066	11
101	76	C	SSI ECL	-	13	5	P	9.3 E7	.041	38
099	77	C	SSI ECL	-	13	5	M	6.8 E7	.038	26
102	77	C	SSI ECL	-	13	5	P	2.5 E8	.029	70
100	78	C	SSI ECL	-	13	5	M	1.0 E8	.035	35
103	78	C	SSI ECL	-	13	5	P	2.5 E8	.021	51
129	76	G	SSI ECL GATE	10102	10	5	M	3.9 E7	.039	
130	77	G	SSI ECL GATE	10102	10	5	M	6 E7	.031	
131	78	G	SSI ECL GATE	10102	10	5	M	7.5 E7	.039	
003	74	A	SSI HTTL	-	10	5	P	1.3 E8	.015	15
011	74	A	SSI HTTL	-	10	5	M	2.0 E7	.0045	0
020	74	A	SSI HTTL	-	10	5	P	7 E8	.003	19
028	74	A	SSI HTTL	-	10	5	M	1.1 E8	.0008	0
270	72	SA	SSI LIN	-	10	0	P	1.0 E7	.028	
271	77	K	SSI LIN	CUSTOM	12	8	P	5.2 E7	.0079	
043	77	B	SSI LN AM PWR	-	17	7	P	4 E7	.05	
080	76	C	SSI LN OP AMP	-	13	5	M	7.7 E8	.051	395
083	76	C	SSI LN OP AMP	-	13	5	P	8.7 E7	.008	59
193	76	H	SSI LN OP AMP	741	17	5	P	3.6 E9	.001	
194	76	H	SSI LN OP AMP	1458	17	5	P	4.0 E9	.002	
041	77	B	SSI LN OP AMP	-	17	7	P	8.1 E9	.05	
081	77	C	SSI LN OP AMP	-	13	5	M	1.5 E9	.050	720
084	77	C	SSI LN OP AMP	-	13	5	P	1.8 E8	.026	139
163	77	G	SSI LN OP AMP	LM741	10	5	P	3 E8	.067	
200	77	H	SSI LN OP AMP	1458	17	5	P	2.0 E8	.010	4
082	78	C	SSI LN OP AMP	-	13	5	M	7.7 E8	.039	304
085	78	C	SSI LN OP AMP	-	13	5	P	1.1 E8	.022	24
120	78	F	SSI LN OP AMP	-	10	5	P	3.4 E6	.027	0
164	78	G	SSI LN OP AMP	LM741	10	5	P	3.9 E8	.087	
162	76	G	SSI LN OP AMP	LM741	10	5	P	3 E8	.101	
220	73	J	SSI LN VLT REG	-	10	5	P	2.8 E9	.011	307
225	75	J	SSI LN VLT REG	-	12	5	P	4.0 E6	.023	0
227	75	J	SSI LN VLT REG	-	12	5	M	4.0 E6	.023	0
080	76	C	SSI LN VLT RG FIX	-	13	5	M	3.3 E7	.090	30
086	76	C	SSI LN VLT RG FIX	-	13	5	M	5.0 E7	.070	35
089	76	C	SSI LN VLT RG FIX	-	13	5	P	4.1 E7	.092	38
153	76	G	SSI LN VLT RG FIX	-	10	5	P	1.47 E7	.127	
042	77	B	SSI LN VLT RG FIX	-	17	7	P	2.2 E9	.11	
087	77	C	SSI LN VLT RG FIX	-	13	5	M	4.5 E7	.002	50
090	77	C	SSI LN VLT RG FIX	-	13	5	P	1.1 E8	.103	112
154	77	G	SSI LN VLT RG FIX	-	10	5	P	1.7 E7	.12	
091	78	C	SSI LN VLT RG FIX	-	13	5	P	7.4 E7	.045	33
155	78	G	SSI LN VLT RG FIX	-	10	5	P	2.7 E7	.073	
092	76	C	SSI LN VLT RG VAR	-	13	5	M	1.2 E8	.122	147
095	76	C	SSI LN VLT RG VAR	-	13	5	P	6.3 E6	.320	20

TABLE D-2 FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK	DEV HRS	%/1KHR	FA
156	76	G	SSI LN VLT RG VAR	-	16	5	H	4.8 E7	.175	
093	77	C	SSI LN VLT RG VAR	-	13	5	H	2.6 E8	.112	296
096	77	C	SSI LN VLT RG VAR	-	13	5	P	1.5 E7	.298	44
157	77	G	SSI LN VLT RG VAR	-	16	5	H	4.5 E7	.17	
094	78	C	SSI LN VLT RG VAR	-	13	5	H	1.2 E8	.100	118
097	78	C	SSI LN VLT RG VAR	-	13	5	P	1.1 E7	.140	16
158	78	G	SSI LN VLT RG VAR		16	5	H	5.9 E7	.124	
224	75	J	SSI LSTTL	-	12	5	P	1.80 E7	.0051	0
232	77	RAC	SSI LSTTL	-	12,13	4	P	1.3 E6	.07	0
170	76	G	SSI LSTTL GATE	74LS00	16	5	P	3.6 E7	.01	
171	77	G	SSI LSTTL GATE	74LS00	16	5	P	1.0 E8	.005	
172	78	G	SSI LSTTL GATE	74LS00	16	5	P	2 E8	.002	
215	73	J	SSI LTTL	-	16	5	P	1.4 E10	.0047	650
002	74	A	SSI STTL	-	16	5	P	1.9 E7	.0049	0
010	74	A	SSI STTL	-	16	5	H	3.0 E6	.026	0
019	74	A	SSI STTL	-	16	5	P	1.1 E8	.0029	2
027	74	A	SSI STTL	-	16	5	H	1.0 E7	.006	0
223	75	J	SSI STTL	-	12	5	P	1.77 E6	.052	0
231	77	RAC	SSI STTL	-	12,13	4	P	6.8 E6	.014	0
236	77	RAC	SSI STTL	-	5	6,10	H	4.4 E6	.021	0
182	76	G	SSI STTL GATE	74S00	16	5	P	3.0 E7	.017	
183	77	G	SSI STTL GATE	74S00	16	5	P	4.5 E7	.018	
184	78	G	SSI STTL GATE	74S00	16	5	P	8.1 E7	.02	
265	72	SBM	SSI TTL	-	12	4	H	1.5 E7	.028	3
266	72	SBM	SSI TTL	-	12	4	H	9.9 E6	.054	4
267	72	SBM	SSI TTL	-	17	4	H	4.7 E6	.043	1
268	72	SBM	SSI TTL	-	12	4	P	3.3 E6	.028	0
269	72	SBM	SSI TTL	-	12	4	P	8.4 E6	.024	1
270	72	SBM	SSI TTL	-	17	4	P	1.5 E7	.022	2
216	73	J	SSI TTL	-	16	5	P	9.1 E9	.0090	807
001	74	A	SSI TTL	-	16	5	P	1.5 E7	.042	5
009	74	A	SSI TTL	-	16	5	H	2.3 E6	.04	0
018	74	A	SSI TTL	-	16	5	P	1.3 E8	.005	5
026	74	A	SSI TTL	-	16	5	H	1.9 E7	.005	0
221	75	J	SSI TTL	-	12	5	P	1.02 E6	.090	0
228	77	K	SSI TTL	-	11	5	P	4.9 E7	.015	6
233	77	RAC	SSI TTL	-	12,13	4	P	5.5 E6	.017	0
239	77	RAC	SSI TTL	-	4	6,10	H	7.4 E7	.0027	1
240	77	RAC	SSI TTL	-	5	3	H	1.7 E7	.012	1
241	77	RAC	SSI TTL	-	6	3	H	5.8 E6	.11	5
242	77	RAC	SSI TTL	-	10	2	H	1.7 E7	.025	3
243	77	RAL	SSI TTL	-	13	7	H	2.6 E6	.036	0
273	72	SA	SSI TTL FF	-	16	6	P	3.2 E8	.022	
117	78	F	SSI TTL FF	-	16	5	P	5.5 E6	.017	0
272	72	SA	SSI TTL GATE	-	16	6	P	1.9 E9	.012	
176	76	G	SSI TTL GATE	7400	16	5	P	3.4 E8	.021	
177	77	G	SSI TTL GATE	7400	16	5	P	3.5 E8	.020	
116	78	F	SSI TTL GATE	-	16	5	P	2.1 E7	.0044	0
178	78	G	SSI TTL GATE	7400	16	5	P	4.6 E8	.03	
104	76	C	SSI/MSI CMOS	-	13	5	H	3.6 E7	.056	20
107	76	C	SSI/MSI CMOS	-	13	5	P	3.5 E8	.029	10

TABLE D-2 FIELD USAGE FAILURE RATE DATA TABULATED BY PART CLASSIFICATION

LN#	YR	SRC	PART CLASS	PART #	SCR	ENV	PK DEV HRS	%/1KHR	FAILS
105	77	C	SSI/MSI CMOS	-	13	5	M 1.1 E8	.033	34
108	77	C	SSI/MSI CMOS	-	13	5	P 6.8 E8	.025	170
106	78	C	SSI/MSI CMOS	-	13	5	M 8.1 E7	.031	25
109	78	C	SSI/MSI CMOS	-	13	5	P 4.1 E8	.024	99
211	73	J	TRANS PWR NPN	-	10	5	P 5.6 E8	.013	68
068	76	C	TRANS PWR NPN	-	13	5	M 2.9 E8	.005	188
071	76	C	TRANS PWR NPN	-	13	5	P 1.9 E8	.077	146
123	76	G	TRANS PWR NPN	T1P31A	10	5	P 6.2 E6	.022	
126	76	G	TRANS PWR NPN	T1P47	10	5	P 1.6E7	.053	
069	77	C	TRANS PWR NPN	-	13	5	M 6.0 E8	.006	390
072	77	C	TRANS PWR NPN	-	13	5	P 3.8 E8	.005	246
124	77	G	TRANS PWR NPN	T1P31A	10	5	P 1.2 E7	.059	
127	77	G	TRANS PWR NPN	T1P47	10	5	P 1.5 E7	.23	
070	78	C	TRANS PWR NPN	-	13	5	M 2.8 E8	.098	274
073	78	C	TRANS PWR NPN	-	13	5	P 1.7 E8	.050	87
125	78	G	TRANS PWR NPN	T1P31A	10	5	P 1.2 E7	.069	
128	78	G	TRANS PWR NPN	T1P47	10	5	P 2.5 E7	.127	
212	73	J	TRANS PWR PNP	-	10	5	P 4.5 E8	.023	100
074	76	C	TRANS PWR PNP	-	13	5	P 6.9 E8	.047	32
077	76	C	TRANS PWR PNP	-	13	5	P 9.7 E8	.058	56
035	77	B	TRANS PWR PNP	2N174	17	7	M 3.6 E9	.03	
075	77	C	TRANS PWR PNP	-	13	5	M 1.5 E8	.055	131
078	77	C	TRANS PWR PNP	--	13	5	P 2.0 E8	.034	68
076	78	C	TRANS PWR PNP	--	13	5	M 7.3 E8	.060	44
079	78	C	TRANS PWR PNP	-	13	5	P 1.1 E8	.036	38
056	76	C	TRANS SS NFET	-	13	5	M 3.57 E8	.028	94
059	76	C	TRANS SS NFET	-	13	5	P 2.1 E8	.081	173
147	76	G	TRANS SS NFET	-	10	5	P 1.1 E8	.131	
150	76	G	TRANS SS NFET	-	10	5	M 8.0 E6	.032	
057	77	C	TRANS SS NFET	-	13	5	M 7.0 E8	.051	356
060	77	C	TRANS SS NFET	-	13	5	P 4.0 E8	.086	339
148	77	G	TRANS SS NFET	-	10	5	P 1.2 E8	.126	
151	77	G	TRANS SS NFET	-	10	5	M 2.0 E7	.005	
058	78	C	TRANS SS NFET	-	13	5	M 4.1 E8	.044	182
061	78	C	TRANS SS NFET	-	13	5	P 2.0 E8	.016	152
149	78	G	TRANS SS NFET	-	10	5	P 1.6 E8	.075	
152	78	G	TRANS SS NFET	-	10	5	M 2.1 E7	.026	
210	73	J	TRANS SS NPN	-	10	5	P 4.6 E9	.010	456
044	76	C	TRANS SS NPN	-	13	5	M 1.44 E9	.025	355
047	76	C	TRANS SS NPN	-	13	5	P 3.6 E9	.017	598
135	76	G	TRANS SS NPN	2N2222	10	5	M 5.3 E7	.022	
138	76	G	TRANS SS NPN	2N2219	10	5	M 7.2 E7	.096	
141	76	G	TRANS SS NPN	2N3439	10	5	M 7.8 E7	.129	
159	76	G	TRANS SS NPN	2N3904	10	5	P 1.4 E9	.024	
188	76	G	TRANS SS NPN	2N5551	10	5	P 5.2 E8	.085	
195	76	H	TRANS SS NPN	-	17	5	P 2.9 E9	.0045	
036	77	B	TRANS SS NPN	-	17	7	P 2 E9	.01	
045	77	C	TRANS SS NPN	-	13	5	M 2.92 E9	.024	703
048	77	C	TRANS SS NPN	-	13	5	P 7.0 E9	.016	1093
136	77	G	TRANS SS NPN	2N2222	10	5	M 7.0 E7	.0215	
139	77	G	TRANS SS NPN	2N2219	10	5	M 8.0 E7	.043	

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